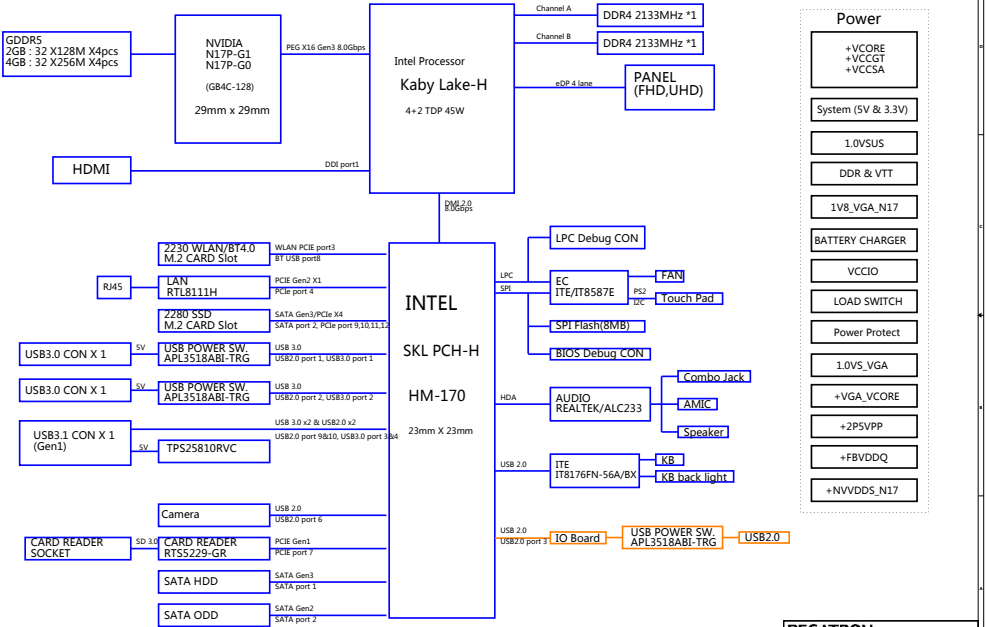
GL553VD Block Diagram



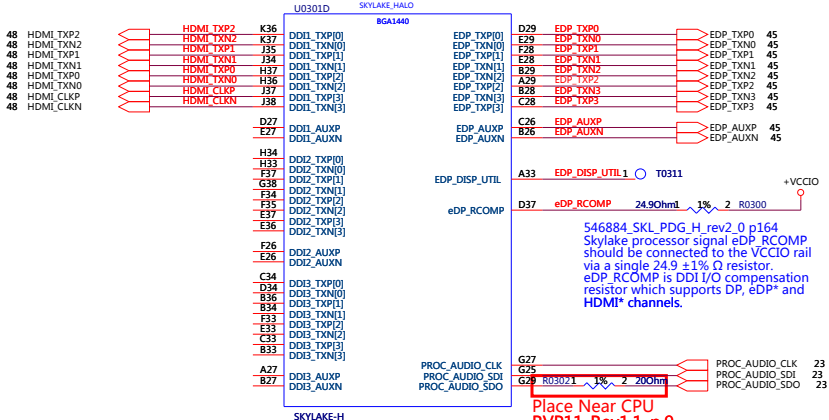
PEGATRON Title : BLOCK DIAGRAM

Engineer: Trunks

Size: Custom | Project Name: GL553VD | Rev: R1.0

Date: Monday, September 11, 2016 | Sheet 1 of 1

3.CPU_DDI/EDP



PEGATRON Title : CPU_DDI/EDP

PEGATRON PROPRIETARY AND CONFIDENTIAL

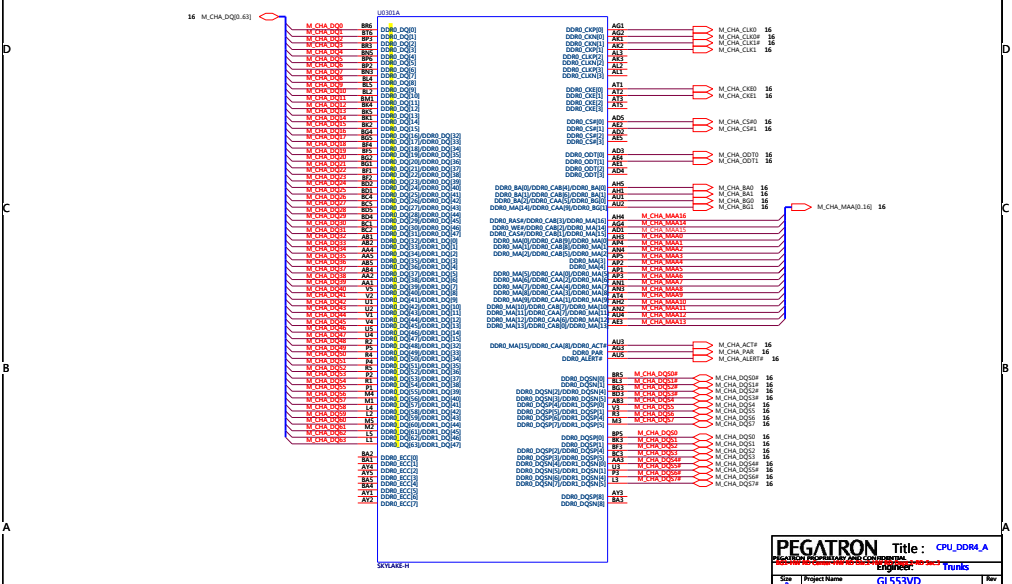
~~IN3-1 HW RD Series 1 HW RD Rev.2 HP RD Rev.2 RD Rev.2 RD Sec.3~~

Engineer: Trunks

Size	Project Name	Rev
A	GL553VD	R2.0

Date: Monday, September 12, 2016 Sheet 3 of 108

04.CPU DDR4 Channel0



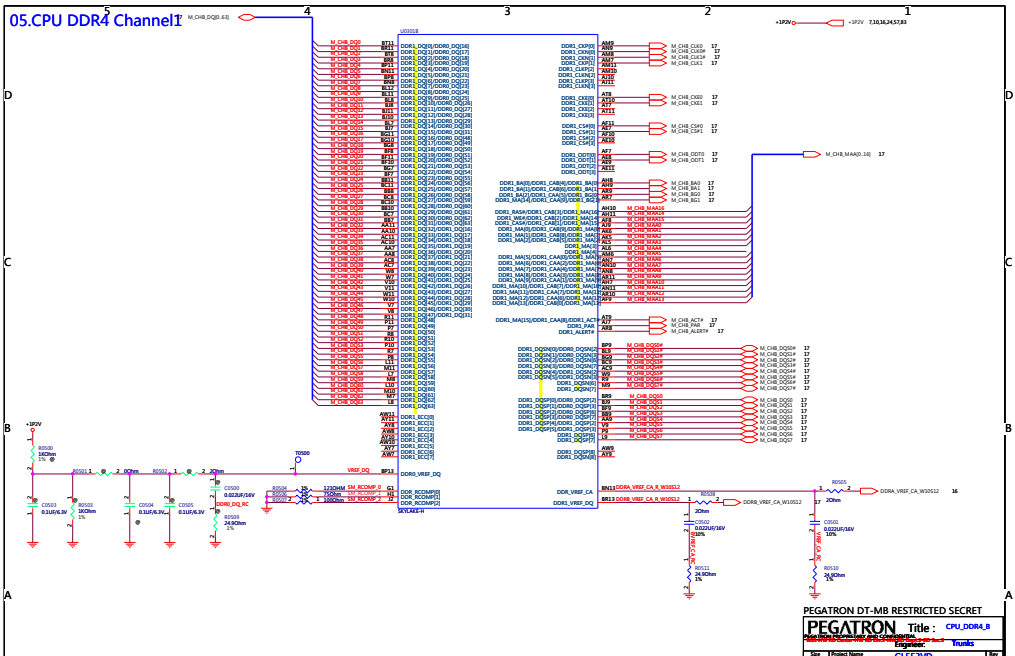
PEGATRON CONFIDENTIAL AND CONFIDENTIAL

Engineer: Trunks

Title : CPU_DDR4_A

Size: B | Project Name: GL553VD | Rev: 3.0

Date: Monday, September 19, 2016 | Sheet 4 of 108


05.CPU DDR4 Channel1
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : CPU_DDR4_8
Engineer: Trunks
GL553VD

06.CPU DMI/PEG

U0301C

+VCCIO ... +VCCIO 3,7,10,94

70 PCIENB_RXN[15:0]
70 PCIENB_RXP[15:0]

PCIEG_TXN[15:0] 70
PCIEG_TXP[15:0] 70

PEG Lane reversal

PCIENB_RXP15	E25	PEG_RXP[0]	PEG_TXP[0]	B25	PCIEG_TXP15_C	C0601	2	1	0.22UF/10V	/VGA	PCIEG_TXP15
PCIENB_RXN15	D25	PEG_RXN[0]	PEG_TXN[0]	A25	PCIEG_TXN15_C	C0602	2	1	0.22UF/10V	/VGA	PCIEG_TXN15
PCIENB_RXP14	E24	PEG_RXP[1]	PEG_TXP[1]	B24	PCIEG_TXP14_C	C0603	2	1	0.22UF/10V	/VGA	PCIEG_TXP14
PCIENB_RXN14	F24	PEG_RXN[1]	PEG_TXN[1]	C24	PCIEG_TXN14_C	C0604	2	1	0.22UF/10V	/VGA	PCIEG_TXN14
PCIENB_RXP13	E23	PEG_RXP[2]	PEG_TXP[2]	B23	PCIEG_TXP13_C	C0605	2	1	0.22UF/10V	/VGA	PCIEG_TXP13
PCIENB_RXN13	D23	PEG_RXN[2]	PEG_TXN[2]	A23	PCIEG_TXN13_C	C0606	2	1	0.22UF/10V	/VGA	PCIEG_TXN13
PCIENB_RXP12	E22	PEG_RXP[3]	PEG_TXP[3]	B22	PCIEG_TXP12_C	C0607	2	1	0.22UF/10V	/VGA	PCIEG_TXP12
PCIENB_RXN12	F22	PEG_RXN[3]	PEG_TXN[3]	C22	PCIEG_TXN12_C	C0608	2	1	0.22UF/10V	/VGA	PCIEG_TXN12
PCIENB_RXP11	E21	PEG_RXP[4]	PEG_TXP[4]	B21	PCIEG_TXP11_C	C0609	2	1	0.22UF/10V	/VGA	PCIEG_TXP11
PCIENB_RXN11	D21	PEG_RXN[4]	PEG_TXN[4]	A21	PCIEG_TXN11_C	C0610	2	1	0.22UF/10V	/VGA	PCIEG_TXN11
PCIENB_RXP10	E20	PEG_RXP[5]	PEG_TXP[5]	B20	PCIEG_TXP10_C	C0611	2	1	0.22UF/10V	/VGA	PCIEG_TXP10
PCIENB_RXN10	F20	PEG_RXN[5]	PEG_TXN[5]	C20	PCIEG_TXN10_C	C0612	2	1	0.22UF/10V	/VGA	PCIEG_TXN10
PCIENB_RXP9	E19	PEG_RXP[6]	PEG_TXP[6]	B19	PCIEG_TXP9_C	C0613	2	1	0.22UF/10V	/VGA	PCIEG_TXP9
PCIENB_RXN9	D19	PEG_RXN[6]	PEG_TXN[6]	A19	PCIEG_TXN9_C	C0614	2	1	0.22UF/10V	/VGA	PCIEG_TXN9
PCIENB_RXP8	E18	PEG_RXP[7]	PEG_TXP[7]	B18	PCIEG_TXP8_C	C0615	2	1	0.22UF/10V	/VGA	PCIEG_TXP8
PCIENB_RXN8	F18	PEG_RXN[7]	PEG_TXN[7]	C18	PCIEG_TXN8_C	C0616	2	1	0.22UF/10V	/VGA	PCIEG_TXN8
PCIENB_RXP7	D17	PEG_RXP[8]	PEG_TXP[8]	A17	PCIEG_TXP7_C	C0617	2	1	0.22UF/10V	/VGA	PCIEG_TXP7
PCIENB_RXN7	E17	PEG_RXN[8]	PEG_TXN[8]	B17	PCIEG_TXN7_C	C0618	2	1	0.22UF/10V	/VGA	PCIEG_TXN7
PCIENB_RXP6	F16	PEG_RXP[9]	PEG_TXP[9]	C16	PCIEG_TXP6_C	C0619	2	1	0.22UF/10V	/VGA	PCIEG_TXP6
PCIENB_RXN6	E16	PEG_RXN[9]	PEG_TXN[9]	B16	PCIEG_TXN6_C	C0620	2	1	0.22UF/10V	/VGA	PCIEG_TXN6
PCIENB_RXP5	D15	PEG_RXP[10]	PEG_TXP[10]	A15	PCIEG_TXP5_C	C0621	2	1	0.22UF/10V	/VGA	PCIEG_TXP5
PCIENB_RXN5	E15	PEG_RXN[10]	PEG_TXN[10]	B15	PCIEG_TXN5_C	C0622	2	1	0.22UF/10V	/VGA	PCIEG_TXN5
PCIENB_RXP4	F14	PEG_RXP[11]	PEG_TXP[11]	C14	PCIEG_TXP4_C	C0623	2	1	0.22UF/10V	/VGA	PCIEG_TXP4
PCIENB_RXN4	E14	PEG_RXN[11]	PEG_TXN[11]	B14	PCIEG_TXN4_C	C0624	2	1	0.22UF/10V	/VGA	PCIEG_TXN4
PCIENB_RXP3	D13	PEG_RXP[12]	PEG_TXP[12]	A13	PCIEG_TXP3_C	C0625	2	1	0.22UF/10V	/VGA	PCIEG_TXP3
PCIENB_RXN3	E13	PEG_RXN[12]	PEG_TXN[12]	B13	PCIEG_TXN3_C	C0626	2	1	0.22UF/10V	/VGA	PCIEG_TXN3
PCIENB_RXP2	F12	PEG_RXP[13]	PEG_TXP[13]	C12	PCIEG_TXP2_C	C0627	2	1	0.22UF/10V	/VGA	PCIEG_TXP2
PCIENB_RXN2	E12	PEG_RXN[13]	PEG_TXN[13]	B12	PCIEG_TXN2_C	C0628	2	1	0.22UF/10V	/VGA	PCIEG_TXN2
PCIENB_RXP1	D11	PEG_RXP[14]	PEG_TXP[14]	A11	PCIEG_TXP1_C	C0629	2	1	0.22UF/10V	/VGA	PCIEG_TXP1
PCIENB_RXN1	E11	PEG_RXN[14]	PEG_TXN[14]	B11	PCIEG_TXN1_C	C0630	2	1	0.22UF/10V	/VGA	PCIEG_TXN1
PCIENB_RXP0	F10	PEG_RXP[15]	PEG_TXP[15]	C10	PCIEG_TXP0_C	C0631	2	1	0.22UF/10V	/VGA	PCIEG_TXP0
PCIENB_RXN0	E10	PEG_RXN[15]	PEG_TXN[15]	B10	PCIEG_TXN0_C	C0632	2	1	0.22UF/10V	/VGA	PCIEG_TXN0

+VCCIO ... R0600 1 1% 2 24.9Ohm PEG_RCOMP G2

PEG_RCOMP

NOTE:
W/S=12/15 mil, length<400mil

20 DMI_RXP0	D8	DMI_RXP[0]	DMI_TXP[0]	B8	DMI_TXP0	20
20 DMI_RXN0	E8	DMI_RXN[0]	DMI_TXN[0]	A8	DMI_TXN0	20
20 DMI_RXP1	E6	DMI_RXP[1]	DMI_TXP[1]	C6	DMI_TXP1	20
20 DMI_RXN1	F6	DMI_RXN[1]	DMI_TXN[1]	B6	DMI_TXN1	20
20 DMI_RXP2	D5	DMI_RXP[2]	DMI_TXP[2]	B5	DMI_TXP2	20
20 DMI_RXN2	E5	DMI_RXN[2]	DMI_TXN[2]	A5	DMI_TXN2	20
20 DMI_RXP3	J8	DMI_RXP[3]	DMI_TXP[3]	D4	DMI_TXP3	20
20 DMI_RXN3	J9	DMI_RXN[3]	DMI_TXN[3]	B4	DMI_TXN3	20

SKYLAKE-H

PEGATRON Title : CPU_DMI

NOT YET RELEASED YET REVISED 2016-09-12 09:09:43 Sec:3

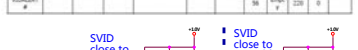
Engineer: Trunks

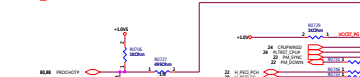
Size	Project Name	Rev
A4	GL553VD	R2.0

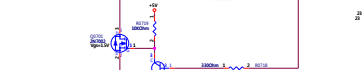
Date: Monday, September 12, 2016 Sheet 6 of 108

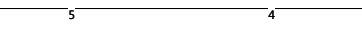
07.CPU MISC

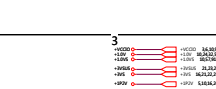
Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W5I [inches]	W5E [inches]	Rpu [Ohm]	Rpu_CPU [Ohm]	Rpu [Ohm]	Rpu [Ohm]	VCCpu [V]
VDDSOUT							100	100	0	10	
VDDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VDDALERT#							56	Empty	220	0	

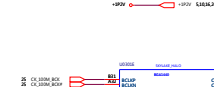


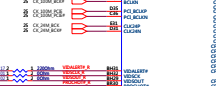


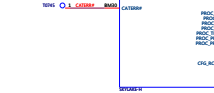


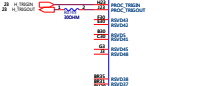


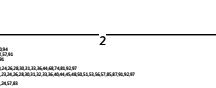


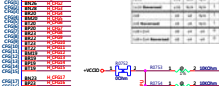


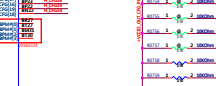


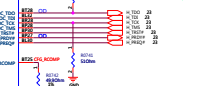


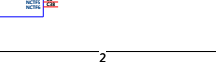






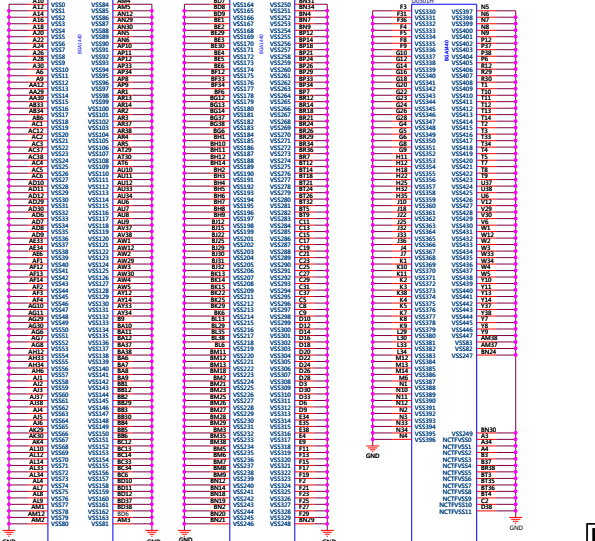






PEGATRON	Title :	CPU_MISC	
	Engineer:	Charles	
Size: B	Project Name: GL553VD		Rev: 1.0
Date: Monday, September 15, 2014	Sheet 7 of 50		

08.CPU VSS

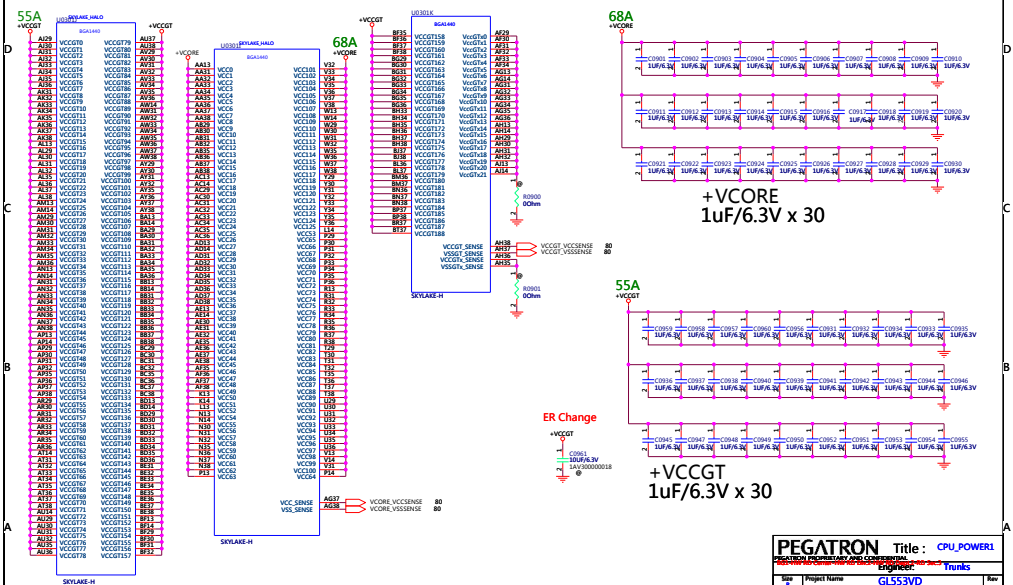


Engineer:	Trunks
Size: B	Project Name: GL553VD
Rev: 2.0	
Date: Monday, September 13, 2016	Sheet: 8 of: 108

PEGATRON Title : CPU_VSS

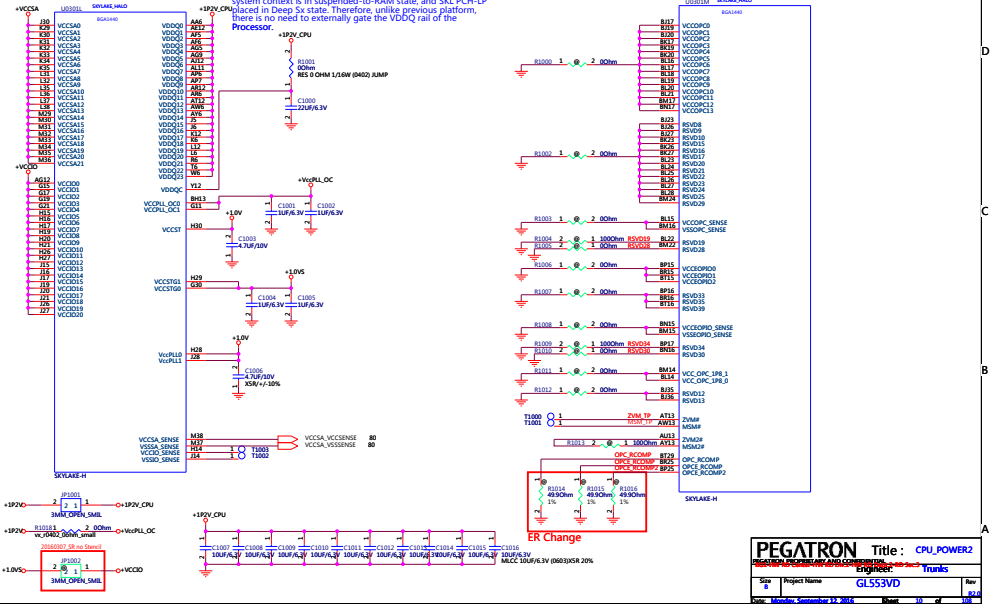
CONFIDENTIAL PROPRIETARY AND CONFIDENTIAL

09.CPU POWER1

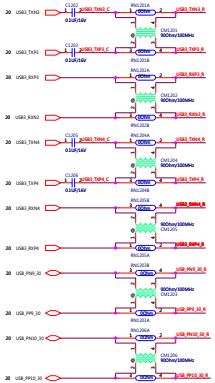


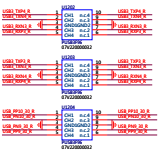
10.CPU POWER2

546884_SKL_PDG_H_rev2_0 (p.622
Skylake processor will internally power gate the VDDQ rail.
system context is in suspended-to-RAM state, and SKL PCH-LP
placed in Deep Sx state. Therefore, unlike previous platform,
there is no need to externally gate the VDDQ rail of the
Processor.



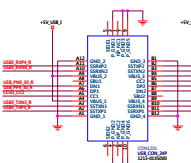
12. Type-C (CC logic,Conn.)



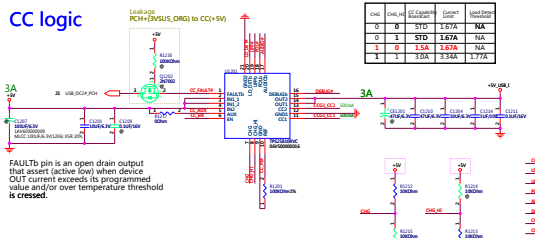


Type-C Conn.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D1+	D1-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU1	D2-	D2+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1



CC logic



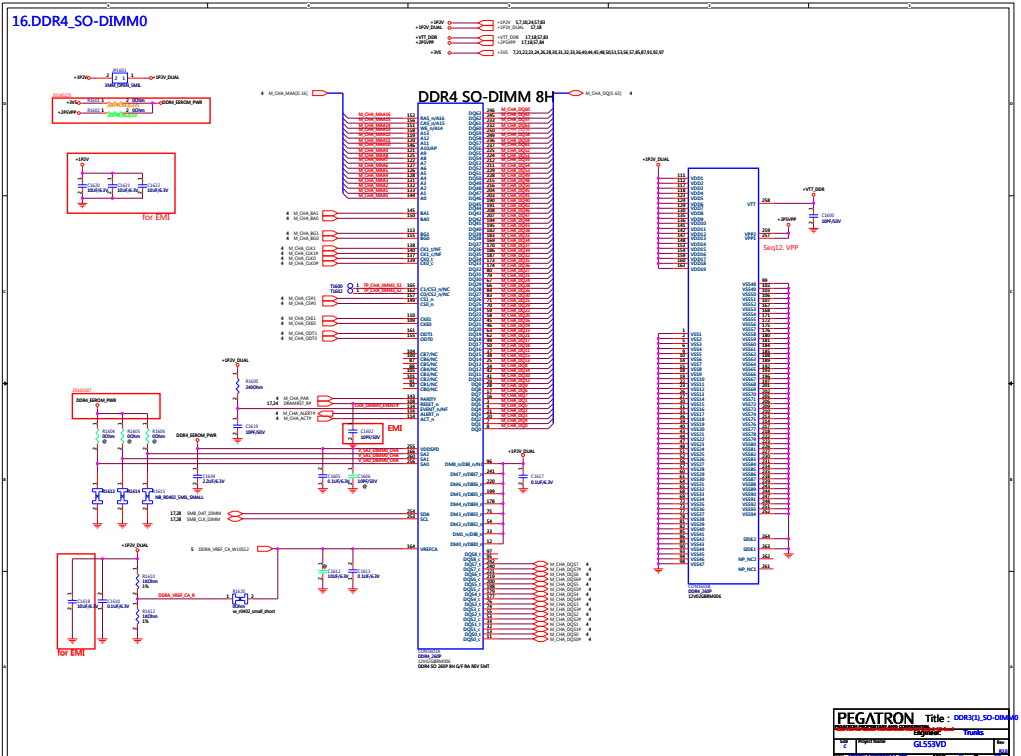
CHG	CHG_HS	CC Capability	Current	Input Power
0	0	STD	1.67A	NA
0	1	STD	1.67A	NA
1	0	1.5A	1.67A	NA
1	1	3.0A	3.34A	1.77A

FAULTb pin is an open drain output that assert (active low) when device OUT current exceeds its programmed value and/or over temperature threshold **is cressed.**

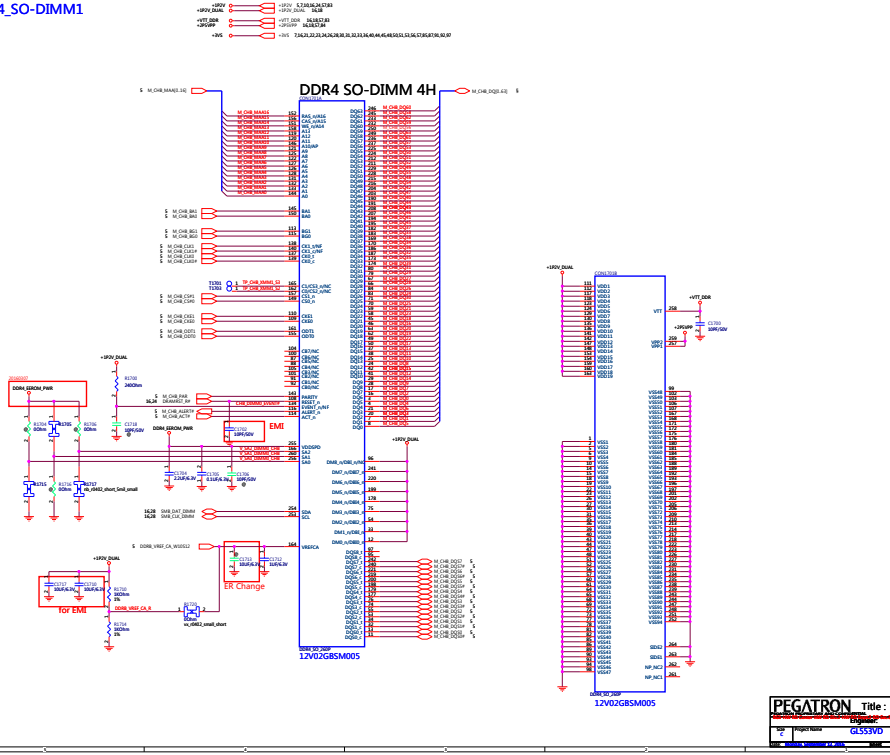
CC_FAULTP	R1250	1	2 100KOhm
I2C_DATP	R1251	1	2 100KOhm
I2CPP	R1260	1	2 100KOhm
PCH_P	R1267	1	2 100KOhm
AUDIOP	R1268	1	2 100KOhm
DEBUGP	R1269	1	2 100KOhm
CC_EN	R1210	1	2 100KOhm

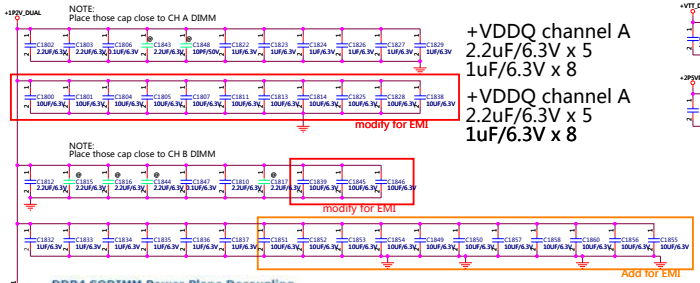
PEGATRON	Title :	Type-C(Conn.)	
Size	Project Name	Rev	
C	GLS53VD	1A1	
Date: Wednesday, February 24, 2016	Sheet 47 of 60		

16.DDR4_SO-DIMM0



17.DDR4_SO-DIMM1

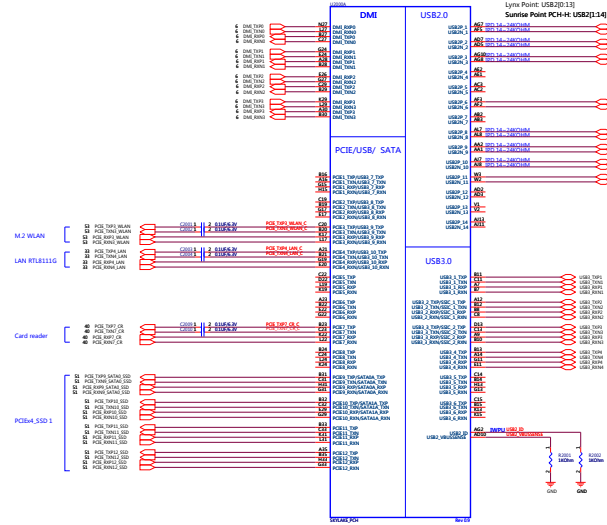




DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 22µF (0402)	

PEGATRON
Title : DDR3 TERMINAL A&B
Engineer: Trunks
Size: B | Project Name: GL553VD | Rev: 3.0
Date: Monday, September 12, 2016 | Sheet 18 of 108



546884_SKL_PDG_H_rev2_0 p233 : HM170 doesn't support PCIE17-20

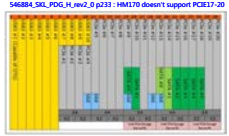


Table 1-3. PCH-H HSIO Detail (Lane 1-14)

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
HM170	USB 3.0 (or GPIO)	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	PCIe	PCIe / LAN	PCIe/ LAN	PCIe	PCIe	PCIe

Table 1-4. PCH-H HSIO Detail (Lane 15-26) (Sheet 1 of 2)

SKU	15[1]	16[1]	17	18	19[1]	20[1]	21	22	23	24	25	26
HM170	PCIe/LAN /SATA0	PCIe/ LAN/ SATA1	PCIe	PCIe/ LAN	PCIe/ LAN/ SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	N/A	N/A	N/A	N/A

PEGATRON CONFIDENTIAL & RESTRICTED SECRET

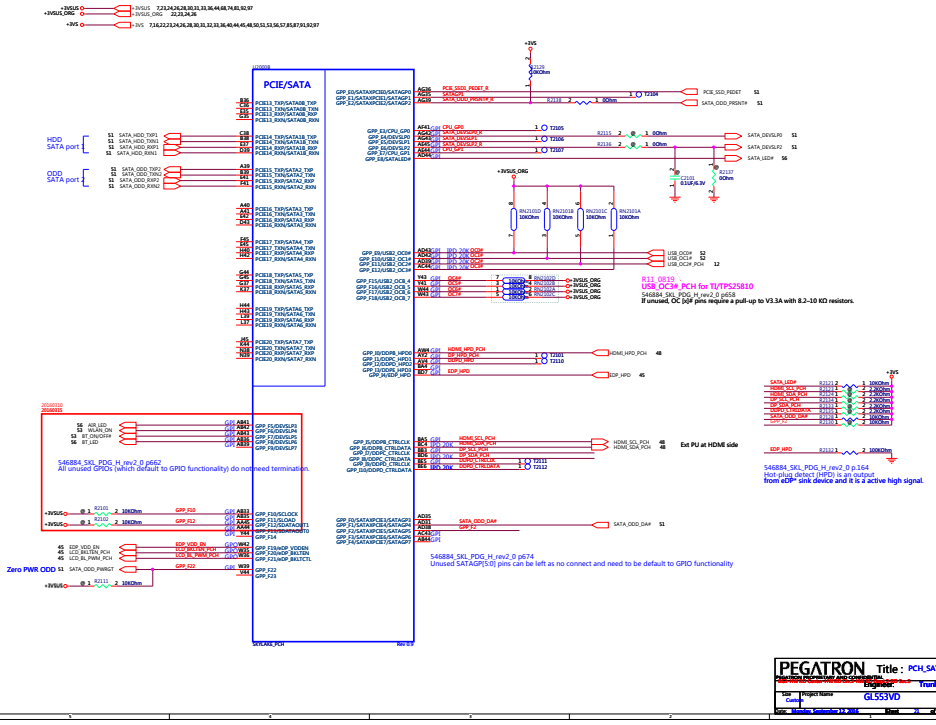
PEGATRON Title : PCH_DMI/PCIE

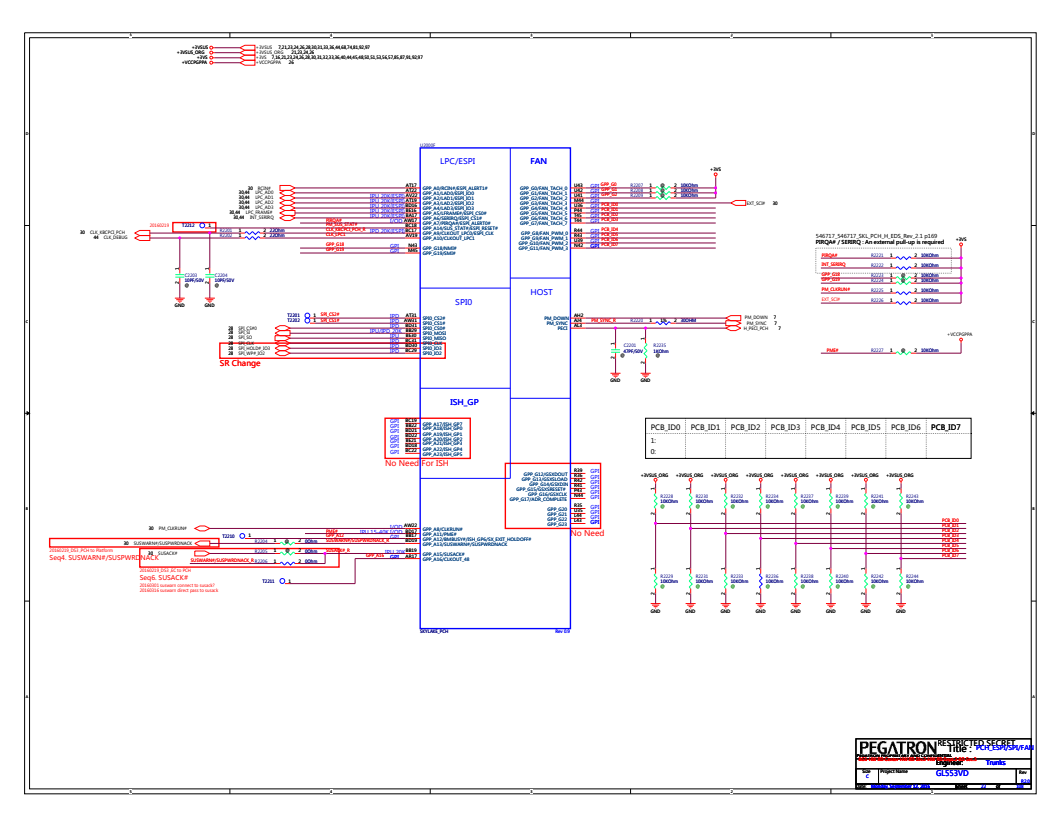
Size: Project Name: GL553VD

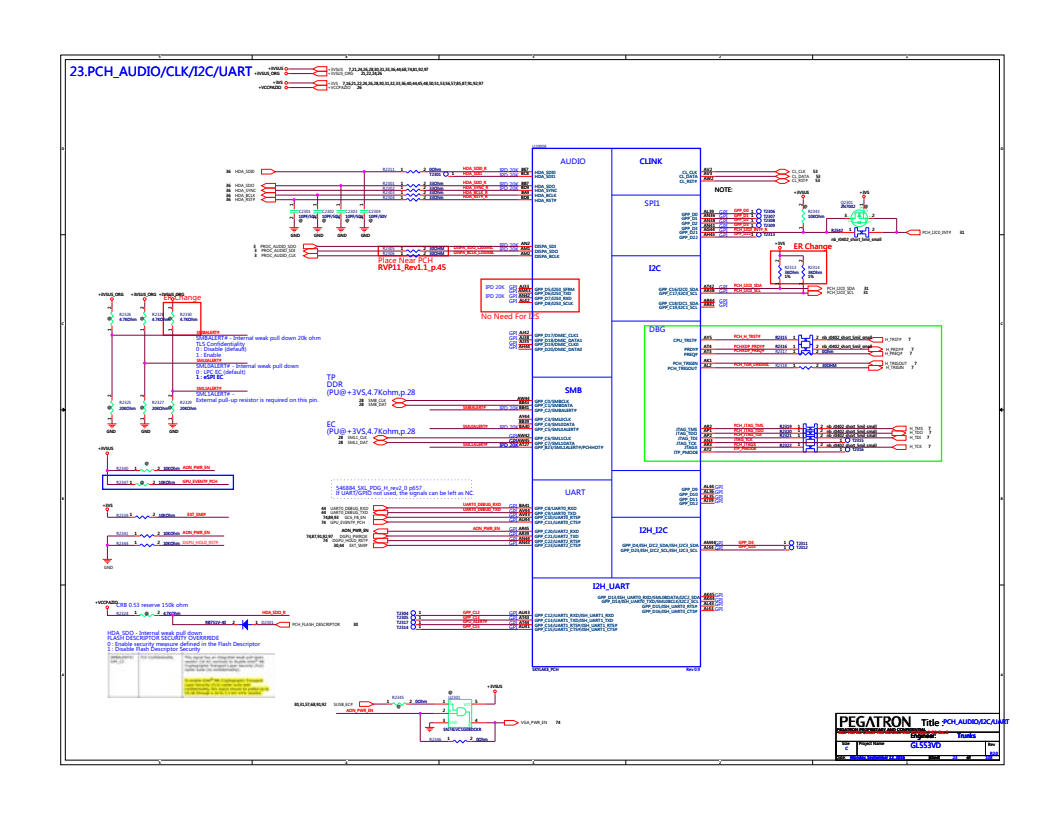
Engineer: Trunks

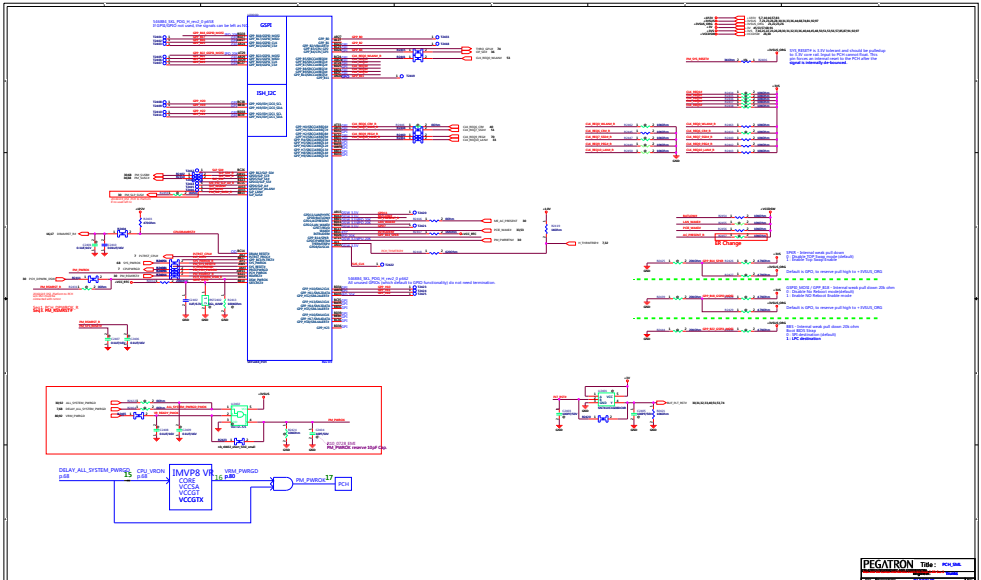
Rev: 1.0

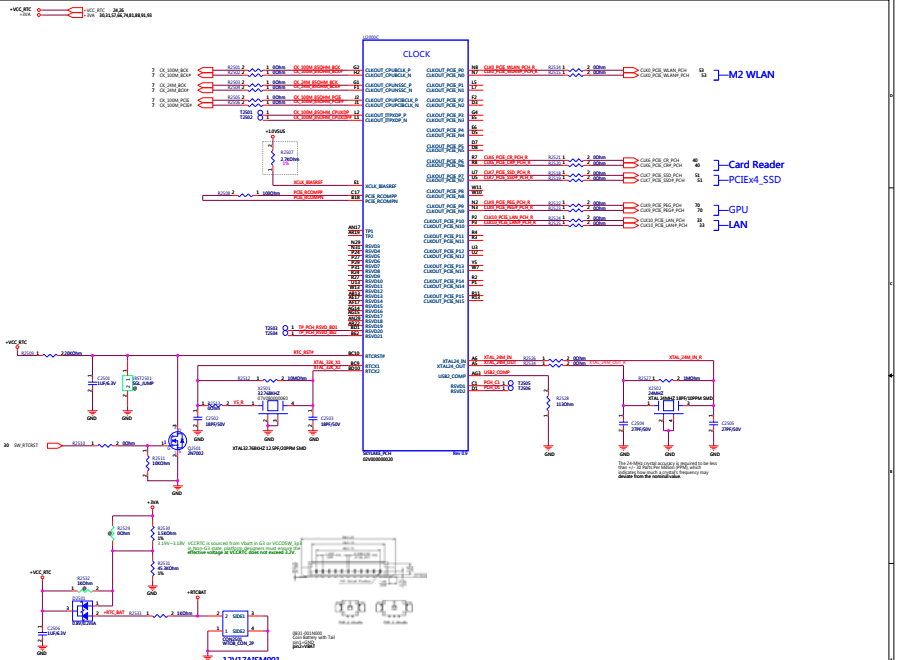
Date: Sheet of

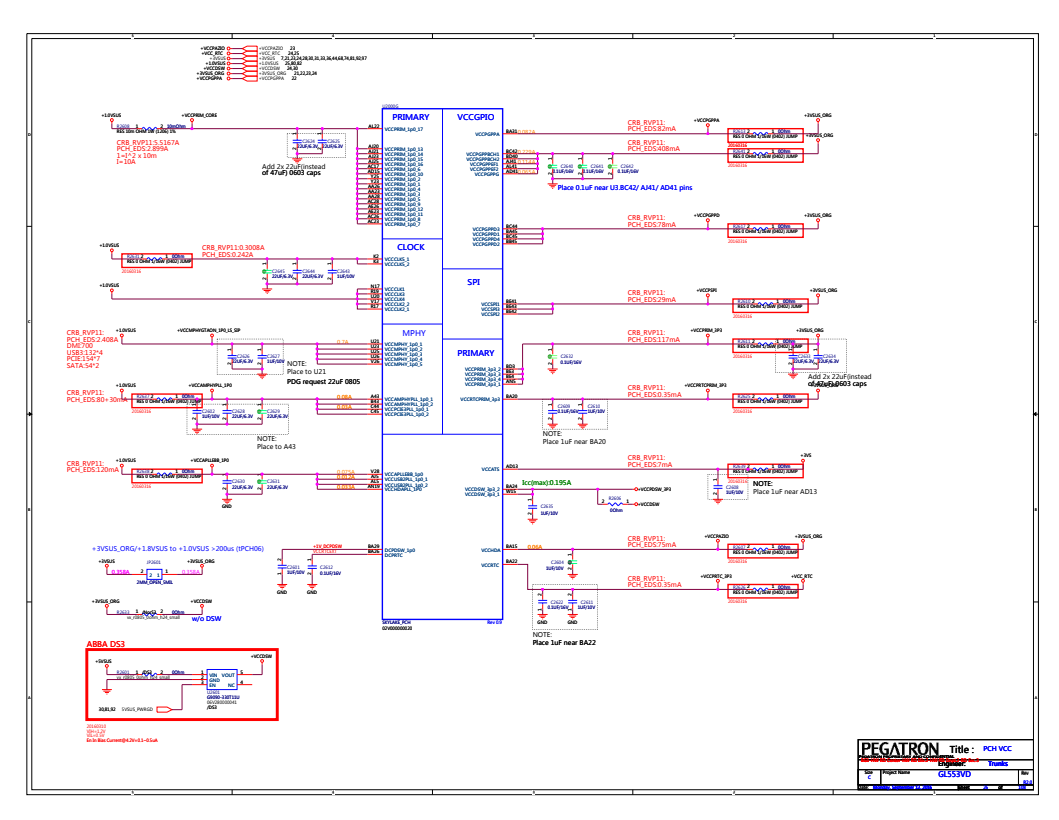

+3VSUS
+3VSUS_ORG
+3VS
PCIE/SATA
HDD SATA port 1
ODD SATA port 1
Zero PWR ODD
SATA_HDD_TXP1
SATA_HDD_TXN1
SATA_HDD_RXP1
SATA_HDD_RXN1
SATA_ODD_TXP2
SATA_ODD_TXN2
SATA_ODD_RXP2
SATA_ODD_RXN2
SATA_ODD_PWRGT
EDP_VDD_EN
LCD_BKLTEN_PCH
LCD_BL_PWM_PCH
GPP_F22
GPP_F10
GPP_F12
SATA_HDD_DAP
SATA_ODD_DAP
HDMI_SCL_PCH
HDMI_SDA_PCH
DP_SCL_PCH
DP_SDA_PCH
HDMI_HPD_PCH
EDP_HPD
SATA_LED#
R113, 0R1/5
USB_OC3# _PCH for TI/TPS25810
546884_SKL_PDG_H_rev2_0 p658
If unused, OC pin pins require a pull-up to V3.3A with 8.2~10 KΩ resistors.
546884_SKL_PDG_H_rev2_0 p664
All unused GPIOs (which default to GPIO functionality) do not need termination.
546884_SKL_PDG_H_rev2_0 p.164
Hot-plug detect (HPD) is an output
from eDP* sink device and it is a active high signal.
546884_SKL_PDG_H_rev2_0 p674
Unused SATAGP[5:0] pins can be left as no connect and need to be default to GPIO functionality
PEGATRON
Title : PCH_SATA/PCIE
Engineer: Trunks
Project Name: GL553VD
Rev: 2.0
Date: Monday, September 19, 2016
Sheet 21 of 105

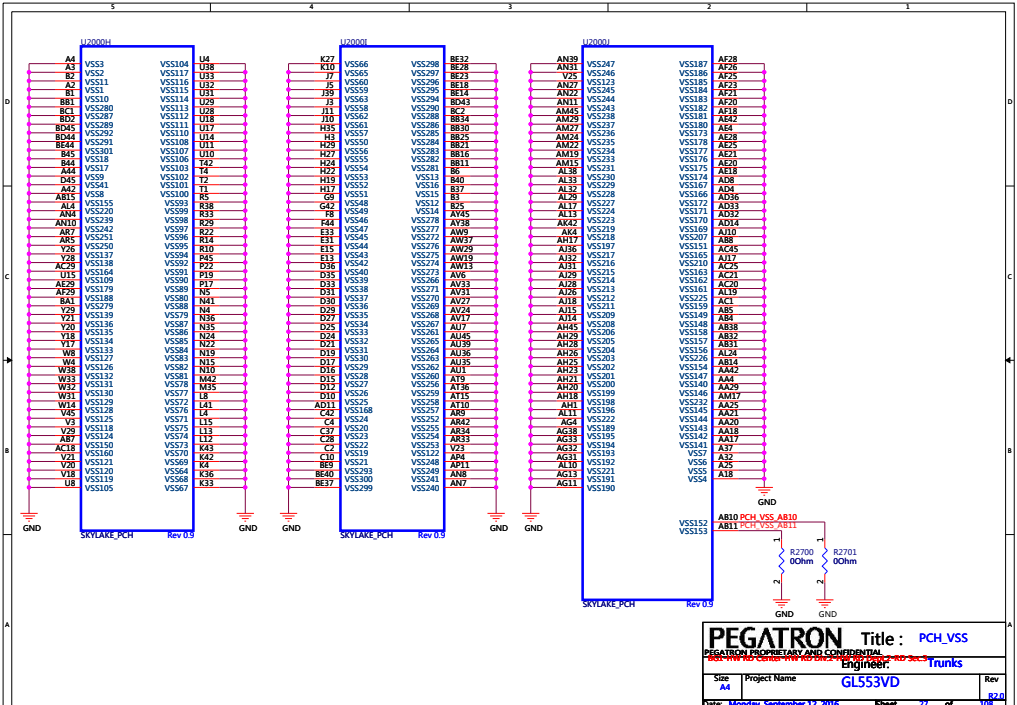

LPC/ESPI
FAN
SPI0
HOST
ISH_GP
SR Change
No Need For ISH
No Need
Seq4. SUSWARN#/SUSPWRDNACK
Seq6. SUSACK#
PCB_ID0
PCB_ID1
PCB_ID2
PCB_ID3
PCB_ID4
PCB_ID5
PCB_ID6
PCB_ID7
PEGATRON
RESTRICTED SECRET
Title : PCH ESPI/SPI/FAN
Engineer :
Trunks
GL553VD
546717_546717_SKL_PCH_H_EDS_Rev_2.1 p169
PIRQA# / SERIRQ : An external pull-up is required


23.PCH_AUDIO/CLK/I2C/UART
AUDIO
CLINK
SPI1
I2C
DBG
SMB
UART
I2H_I2C
I2H_UART
NOTE:
ER Change
Place Near PCH
RVP11_Rev1.1_p.45
No Need For ES
TP
DDR
(PU@+3VS,4.7Kohm,p.28
EC
(PU@+3VS,4.7Kohm,p.28
546884_SKL_PDG_H_rev2_0 p657
If UART/GPIO not used, the signals can be left as NC.
HDA_SDO : Internal weak pull down
FLASH DESCRIPTOR SECURITY OVERRIDE
0 : Enable security measure defined in the Flash Descriptor
1 : Disable Flash Descriptor Security
PEGATRON
Title :PCH_AUDIO/I2C/UART
Engineer:
Trunks
Project Name:
GL553VD
Rev:
1.0
Size:
C
Date:
Sheet
of


GSPI
ISH_I2C
IMVP8 VR
CORE
VCCSA
VCCIO
VCCGTX
DELAY_ALL_SYSTEM_PWRGD
CPU_VRON
VRM_PWRGD
PM_PWROK
PCH
PEGATRON
Title : PCH_SML
Size : Document Number : Rev
Date : Sheet of


CLOCK
M2 WLAN
Card Reader
PCIEx4_SSD
GPU
LAN
12V17AISM001
PEGATRON
Title : PCH_CLOCK
Engineer: Trunks
GL553VD


PRIMARY
VCCGPIO
CLOCK
SPI
MPHY
PRIMARY
CRB_RVP11: PCH_EDS:82mA
CRB_RVP11: PCH_EDS:40mA
CRB_RVP11: PCH_EDS:78mA
CRB_RVP11: PCH_EDS:29mA
CRB_RVP11: PCH_EDS:117mA
CRB_RVP11: PCH_EDS:0.35mA
CRB_RVP11: PCH_EDS:7mA
CRB_RVP11: PCH_EDS:75mA
CRB_RVP11: PCH_EDS:0.35mA
CRB_RVP11: PCH_EDS:2.408A
CRB_RVP11: PCH_EDS:80+:301mA
CRB_RVP11: PCH_EDS:120mA
CRB_RVP11:0.3008A
PCH_EDS:0.242A
Place 0.1uF near U3.BC42/ AJ41/ AD41 pins
Add 2x 22uFinstead of 47uF) 0603 caps
Add 2x 22uFinstead of 47uF) 0603 caps
PDG request 22uF 0805
Place to U21
Place to A43
Place 1uF near BA20
Place 1uF near AD13
Place 1uF near BA22
Icc(max):0.195A
0.05A
+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (tPCH06)
w/o DSW
ABBA DS3
PEGATRON
Title : PCH VCC
Engineer: Trunks
Project Name
GL553VD
Rev
1.0



PEGATRON Title : PCH_VSS

PEGATRON PROPRIETARY AND CONFIDENTIAL

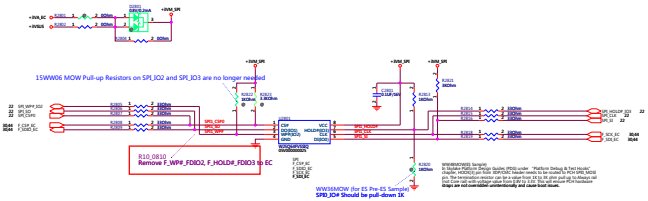
Engineer: Trunks

Size	Project Name	Rev
A4	GL553VD	R2.0

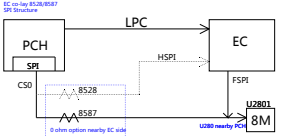
Date: Monday, September 12, 2016 Sheet 27 of 108

28.SPI ROM/SMbus

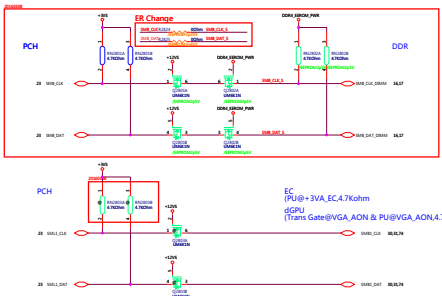
SPI ROM



EC co-lay 8528/8587
SPI Structure



SMBus

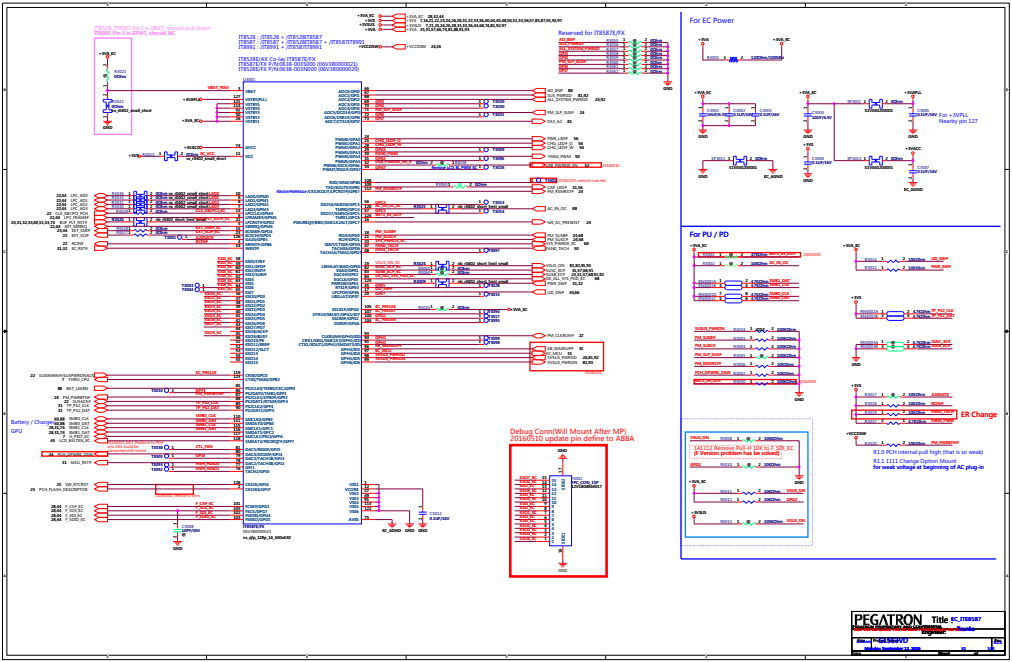


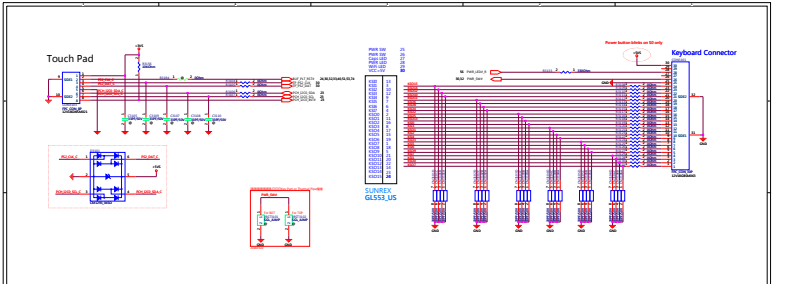
PEGATRON Title : SPI ROM/SMbus

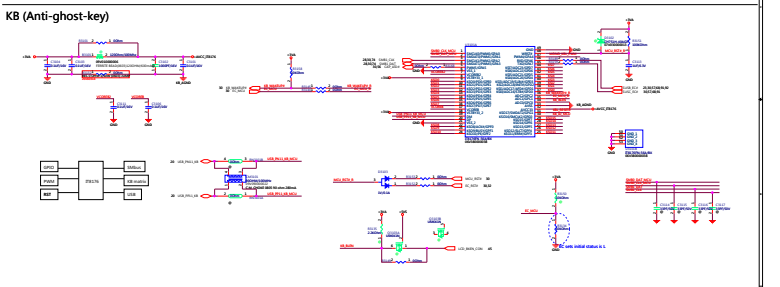
Engineer: Tsunda

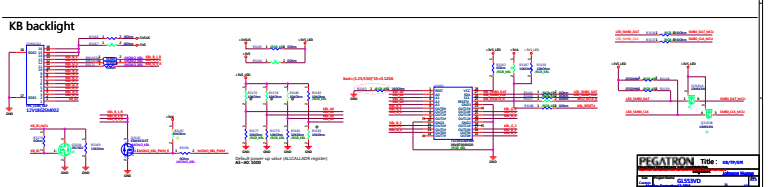
Size: A3 | Project Name: GL553VD | Rev: 3.0

Date: Monday, November 23, 2015 | Sheet 28 of 58

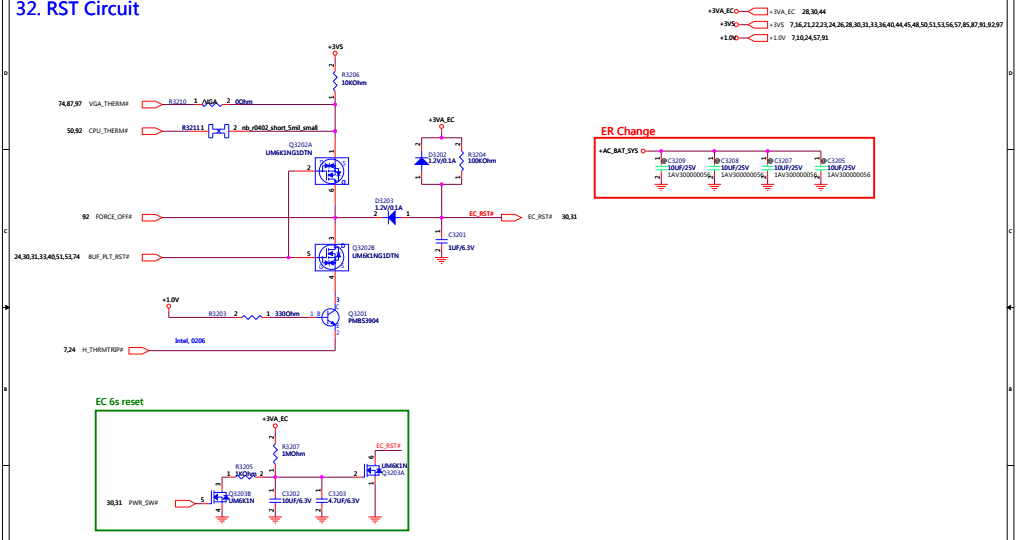

For EC Power
For PU / PD
Debug Conn(Will Mount After MP)
20160510 update pin define to ABBA
ER Change
Battery / Charger
GPU
PEGATRON
Title
Engineer:


Touch Pad
Keyboard Connector
SUNREX
GL553_US


KB (Anti-ghost-key)


KB backlight
PEGATRON
Title :
GL553VD

32. RST Circuit



+3VA_EC +3VA_EC 28,30,44

+3VS +3VS 7,16,21,22,23,24,26,28,30,31,33,36,40,44,45,48,50,51,53,56,57,85,87,91,92,97

+1.0V +1.0V 7,10,24,57,91

ER Change

EC 6s reset

PEGATRON Title : 32. RST Circuit

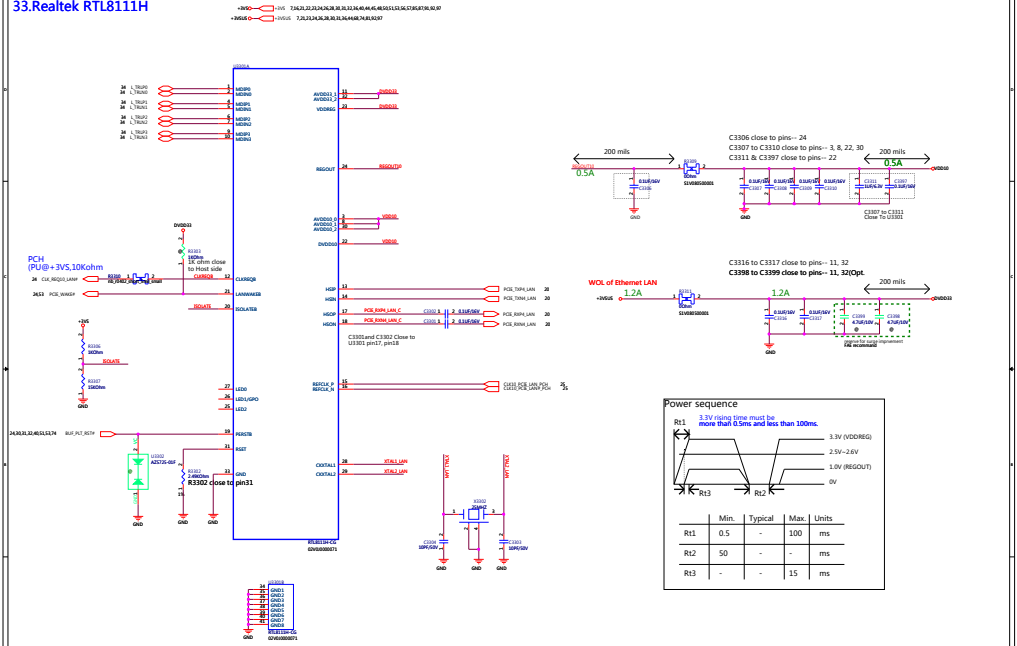
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Chunks

Size	Project Name	Rev
B	GL553VD	2.0

Date: Monday, September 12, 2016 Sheet 32 of 101

33.Realtek RTL8111H



C3306 close to pins-- 24
C3307 to C3310 close to pins-- 3, 8, 22, 30
C3311 & C3397 close to pins-- 22

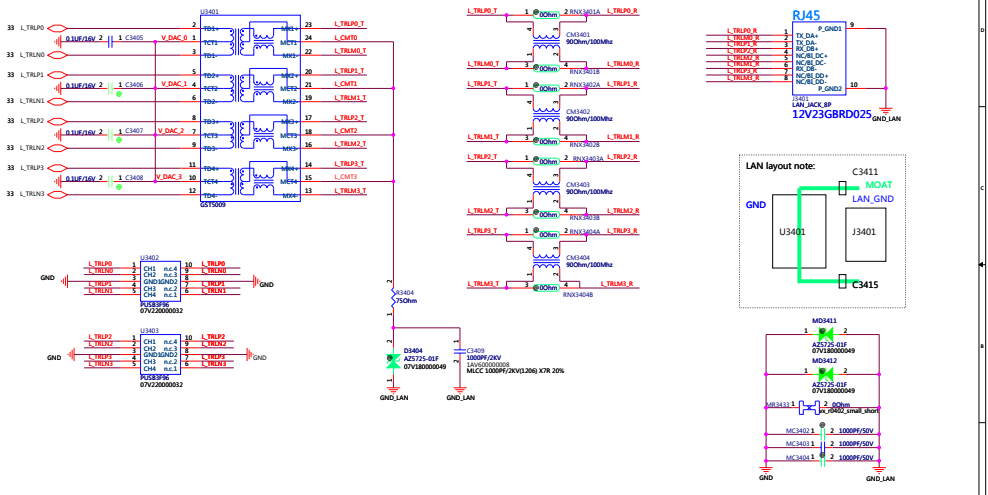
C3316 to C3317 close to pins-- 11, 32
C3398 to C3399 close to pins-- 11, 32(Opt.

Power sequence

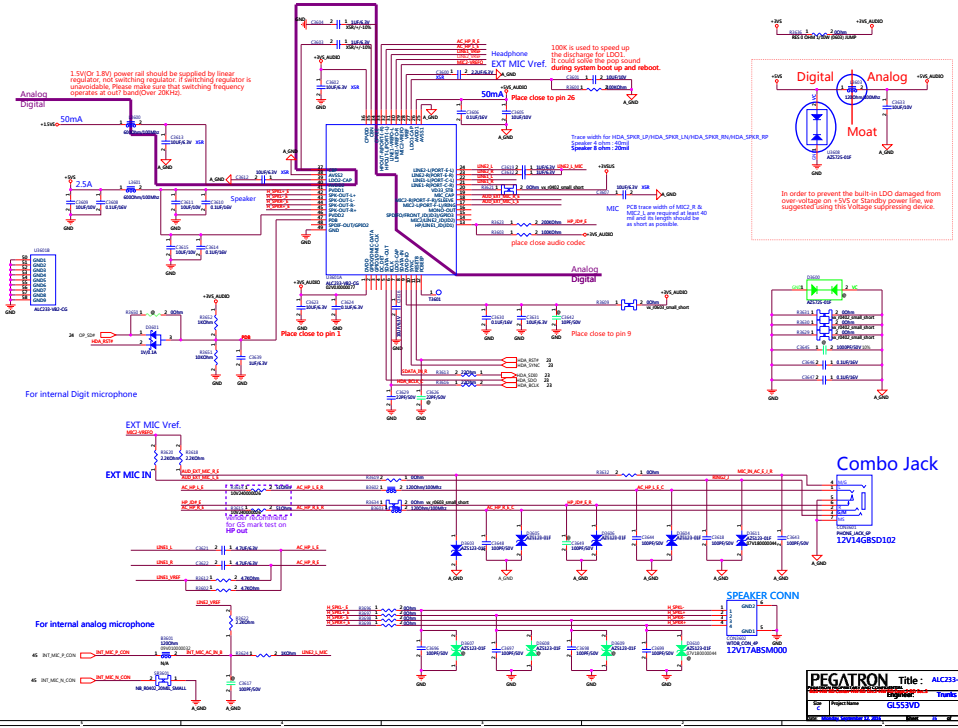
	Min.	Typical	Max.	Units
Rt1	0.5	-	100	ms
Rt2	50	-	-	ms
Rt3	-	-	15	ms

PEGATRON Title : Realtek RTL8111H
Engineer: Tramis
Size: D | Project Name: GL5S3VD | Rev:
Date: Sheet of

34.Transformer/RJ45

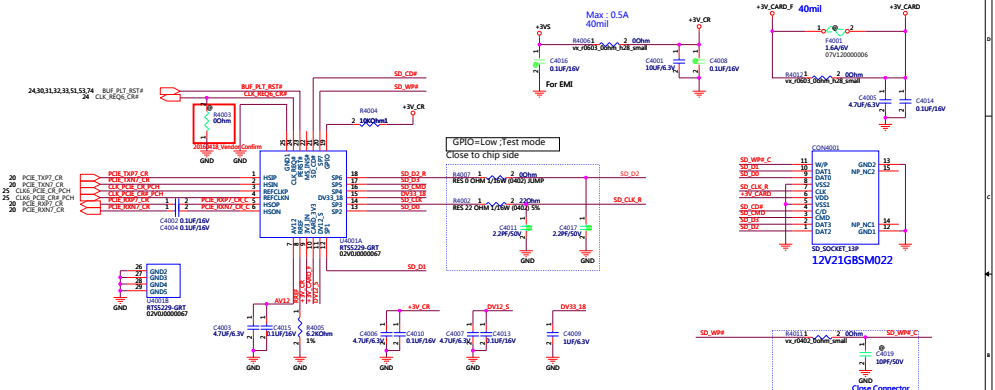


ALC233-VB2-CG CODEC



PEGATRON	Title :	ALC233- CODEC	
	Engineer:	Trunks	
Size	Project Name	GL553VD	Rev
			1.0
Date: Monday, November 23, 2015		Sheet 26 of 37	

Cardreader



Pin Name	Description
SP1	SDWP# / MSCLK
SP2	MS_INS#
SP3	SD_DAT1
SP4	SD_DAT0
SP5	MS_D3
SP6	SD_CD#
SP8	SD_CLK / MS_D2
SP9	MS_D0
SP10	SD_CMD
SP12	SD_DAT3 / MS_D1
SP13	SD_DAT2
SP14	MS_BS

SP1	SD_WP#	MMC_RSVD
SP3	SD_D1	
SP4	SD_D0	MMC_DAT
SP6	SD_CD#	
SP8	SD_CLK	MMC_CLK
SP10	SD_CMD	MMC_CMD
SP12	SD_D3	
SP13	SD_D2	

PEGATRON Title : RTS5138-GR

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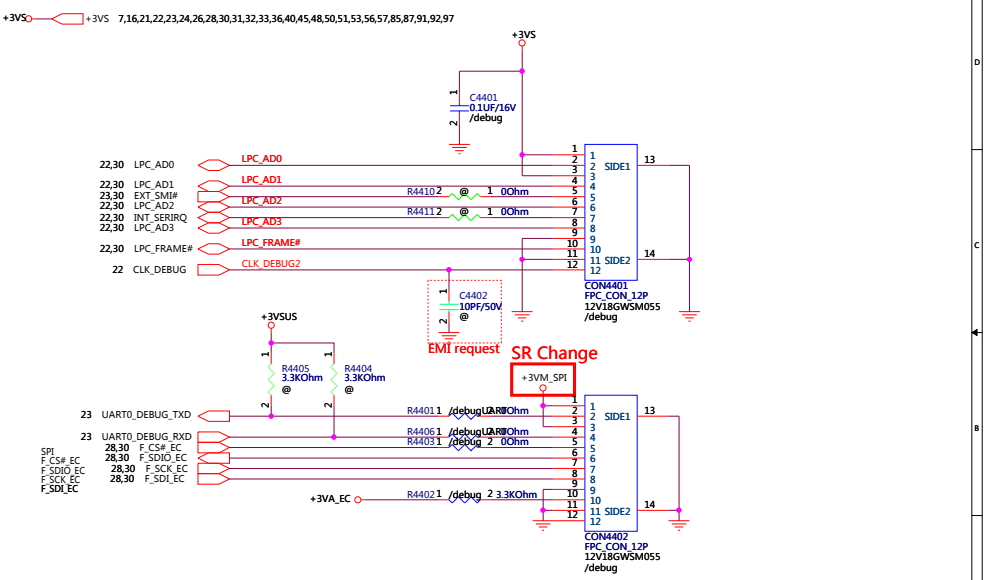
Engineer: Trunks

Size	Project Name	Rev
B	GL553VD	2.0

Date: Monday, September 12, 2016 Sheet 40 of 110



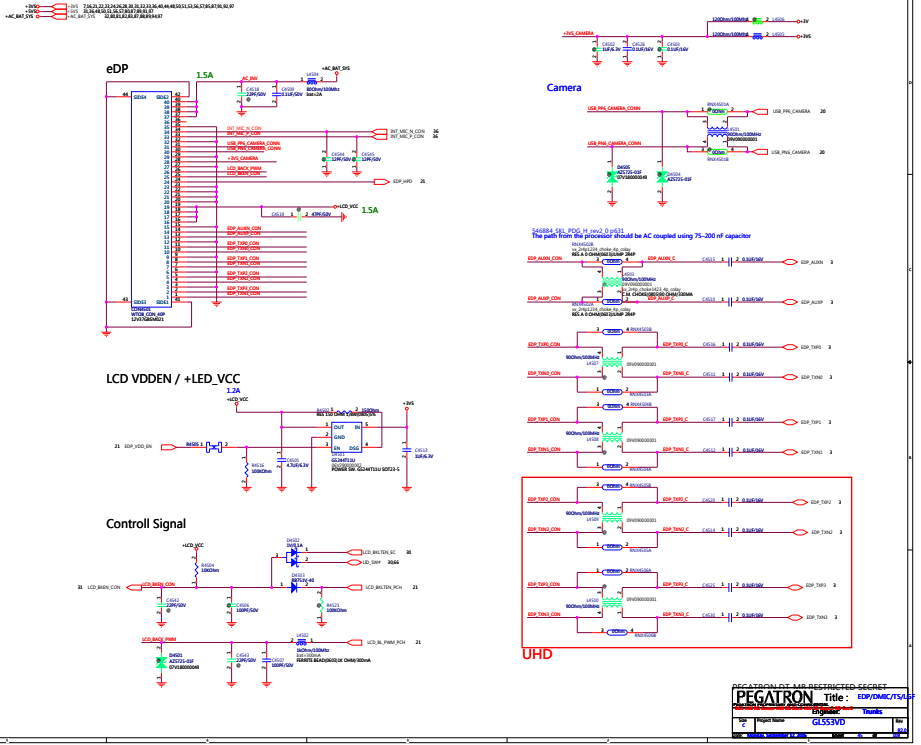
PEGATRON Title : DEBUG CON

PEGATRON PROPRIETARY AND CONFIDENTIAL

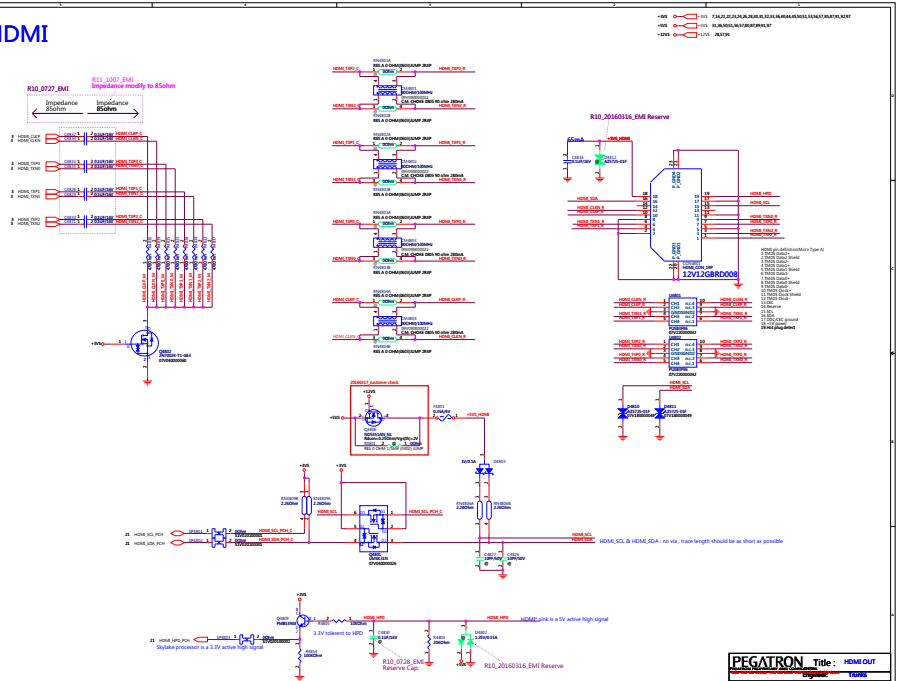
Engineer: Trunks

Size	Project Name	Rev
A	GL553VD	R2.0

Date: Monday, September 12, 2016 Sheet 44 of 108

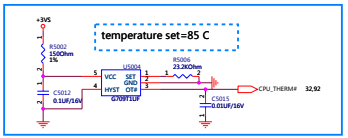

eDP
1.5A
Camera
LCD VDDEN / +LED_VCC
1.2A
Controll Signal
UHD
Title : EDP/DMIC/TS/LS
GL553VD

HDMI

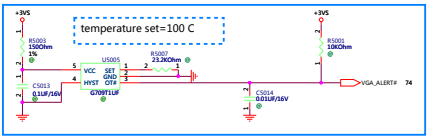


PEGATRON	Title :	HDMI OUT
	Engineer:	Thomas
	Project Name:	GL553VD
	Rev:	3.0

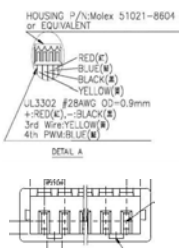
CPU Thermal Sensor



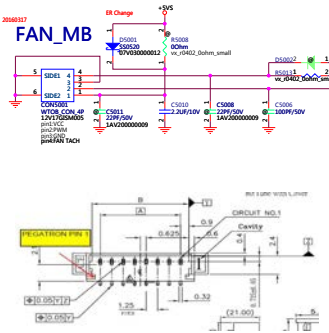
GPU Thermal Sensor



FAN_Module



FAN_MB



PEGATRON	Title :	FAN/THERMAL
PEGATRON PROPRIETARY AND CONFIDENTIAL		
Engineer:	Trunks	
Size: B	Project Name: GL553VD	Rev: 1A.0
Date: Monday, September 12, 2016	Sheet 30 of 38	

NGFF socket M
PCIEx4 SSD1

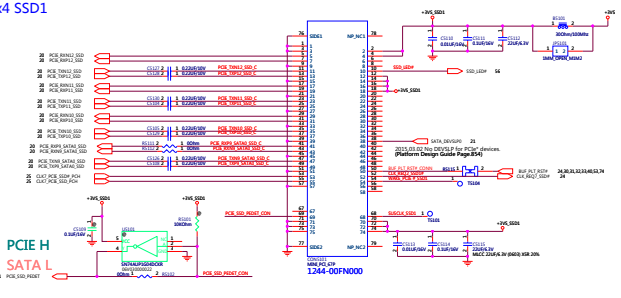
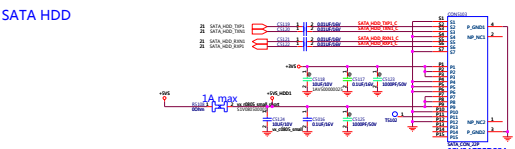
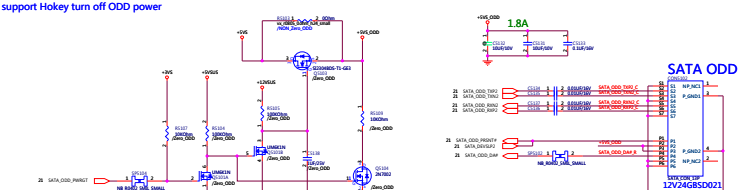


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

SATA HDD

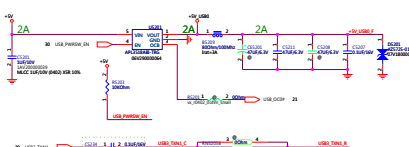


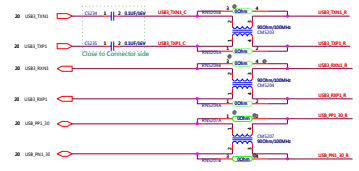
support Hokey turn off ODD power

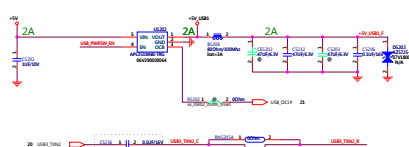


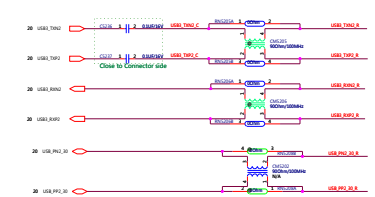
PEGATRON Title : SATA/ODD/SSD
Engineer: Trunks
Project Name: GL55SVD

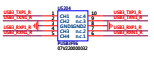
52.USB3.0

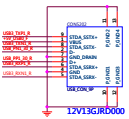


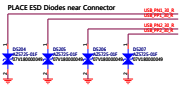


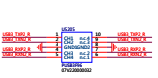


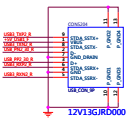












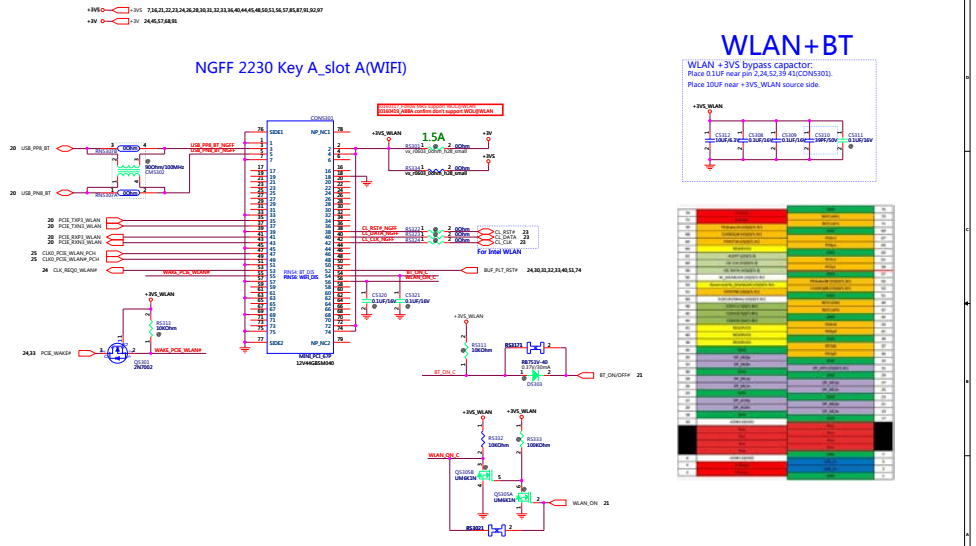
PEGATRON CONFIDENTIAL SECRET

PEGATRON Title : USB3 Port

Engineer: Tsunks

Size	Project Name	Rev
A	GL553VD	1A

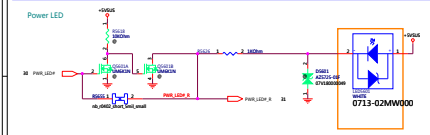
Date: Monday, September 07, 2015 Sheet 52 of 60


NGFF 2230 Key A_slot A(WIFI)
WLAN+BT
WLAN +3VS bypass capactor:
Place 0.1UF near pin 2,24,52,39 41(CON5301).
Place 10UF near +3VS_WLAN source side.
+3VS_WLAN
CS312 10UF/6.3V
CS308 0.1UF/16V
CS309 0.1UF/16V
CS310 10PF/50V
CS311 0.1UF/16V
1.5A
+3VS_WLAN
+3V
+3VS
CON5301
NP_NC1
NP_NC2
SIDE1
SIDE2
MINI_PCI_E5P
12V44GB504040
USB_PP8_BT
USB_PN8_BT
USB_PP8_BT_NGFF
USB_PN8_BT_NGFF
RN5301
RN5302
90Ohm/100MHz
CM5302
PCIE_TXP2_WLAN
PCIE_TXN2_WLAN
PCIE_RXP2_WLAN
PCIE_RXN2_WLAN
CLK0_PCIE_WLAN_PCH
CLK0_PCIE_WLAN#_PCH
CLK_REQ0_WLAN#
WAKE_PCIE_WLAN#
RN54 8T_D/S
RN56 WIFI_D/S
BC_I2C_C
WCAN_I2C_C
CS320 0.1UF/16V
CS321 0.1UF/16V
+3VS_WLAN
RS3221 2.0Ohm
RS3222 2.0Ohm
RS3223 2.0Ohm
CL_RST# 23
CL_DATA 23
CL_CLK 23
For Intel WLAN
BUF_PLT_RST# 24,30,31,32,33,40,51,74
+3V_WLAN
RS3211 10KOhm
RS3171
BT_ON_C
BT_ON/OFF# 21
DA488
+3VS_WLAN
+3VS_WLAN
RS332 10KOhm
RS333 100KOhm
WLAN_ON_C
QS305B UM6K3N
WLAN_ON 21
RS3021
+3V_WLAN
RS322 10KOhm
QS303 2N7002
24,33 PCIE_WAKE#
WAKE_PCIE_WLAN#
PEGATRON
Title : NGFF_WLAN
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Trunks
Size Project Name GL553VD Rev
Custom
Date: Monday, September 14, 2015 Sheet 34 of 81

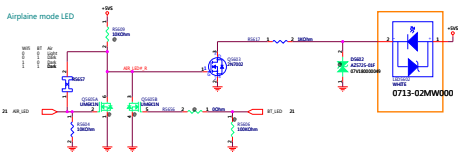
+5VSUS 26,31,51,81

+5VS 31,34,48,50,51,57,80,87,88,91,97

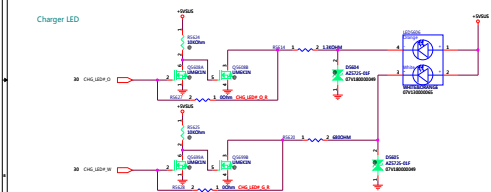
Power LED



Airplaine mode LED

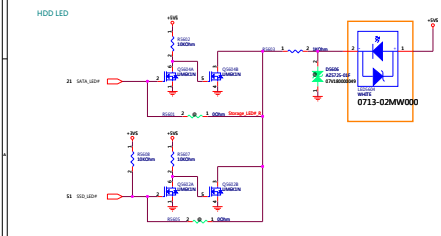


Charger LED



Caps Lock LED

HDD LED



MB LED Placement

Left-->Right

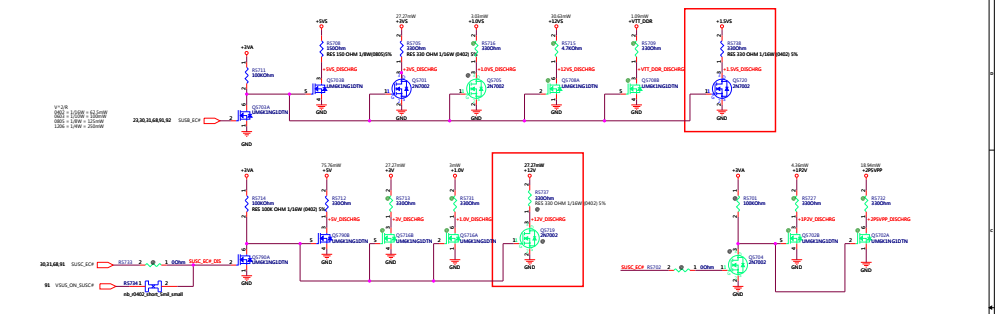
PWR LED	Charger LED	HDD LED	RF LED	Caps Lock LED
LED5601	LED5606	LED5604	LED5602	LED5603

Title : PWR BOARD CON

Engineer: Trunks

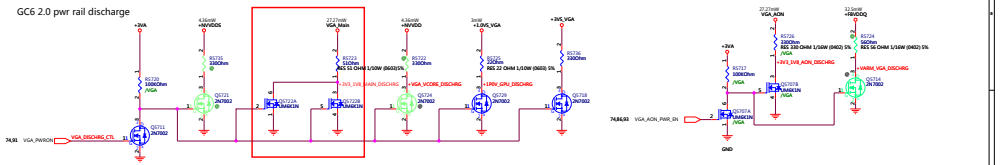
Size	Project Name	Rev
A	GL553VD	

Date: Sheet of



all MOS mount for GPU Optimus function

GC6 2.0 pwr rail discharge



PEGATRON Title : Discharge

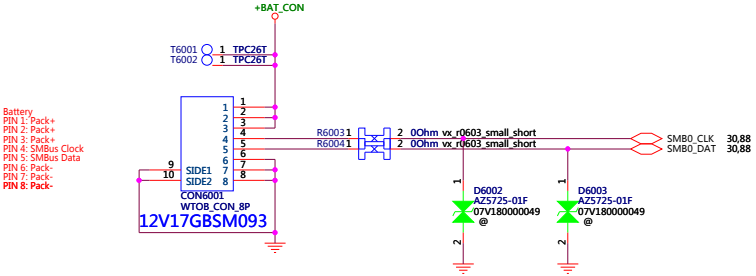
Engineer: Trunks

Size	Project Name	Rev
Custom	GL553VD	2G0

Date: Tuesday, November 10, 2015 Sheet 62 of 100

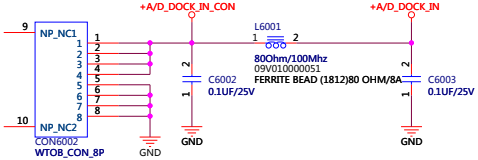
60.BATT CON/AC IN

BATTERY CONNECTOR



AC IN CONNECTOR

Adaptor
120W



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : BATT CON/AC IN

Engineer: Trunks

Size	Project Name	Rev
A	GL553VD	R2.0

Date: Monday, September 12, 2016 Sheet 60 of 108

65.NUT,Screw hole,Tooling hole

CPU NUT

GPU NUT

PCH NUT

Hall Sensor Brd NUT

SSD NUT

NPTH_2.5phi

NPTH_4 x 2.5 phi

ER Change

NPTH_8phi

NPTH_2.5 x 2.9 phi

TYPE A
phi 8 drill 3

TYPE
T_S8 drill3,B_phi8 drill3
T-SH00004213

TYPE
T_phi10 drill3,B_phi8 drill3
ST394CB314D118

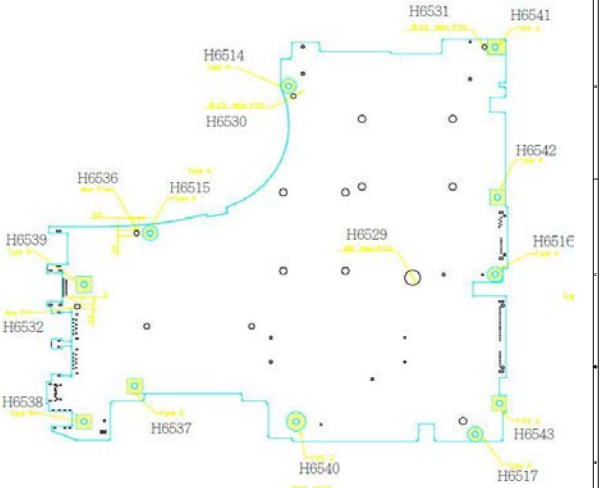
TYPE E(BOT) TYPEB(TOP)
T_s8 drill3,B_R10x8 drill3
RT314RB393x314D118

TYPE G
T_9p5 x 8 drill3,B_phi8 drill3
RT374x314CB314D118

TYPE
phi 6p5 drill 3

ER Change

TYPE D(BOT) TYPE F(TOP)
T_s7p55 drill3,B_R10x8 drill3
RT297X315RBD118



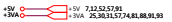
PEGATRON Title : Screw hole

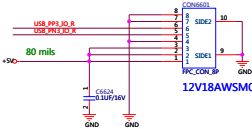
Engineer: Trunks

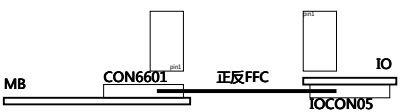
Size: A | Project Name: GL553VD | Rev: 1.0

Date: Monday, September 19, 2016 | Sheet: 65 of 68

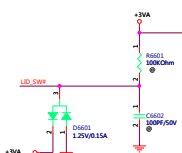
IO BD CONN. (MB SIDE)

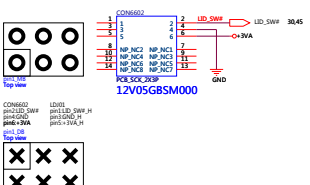




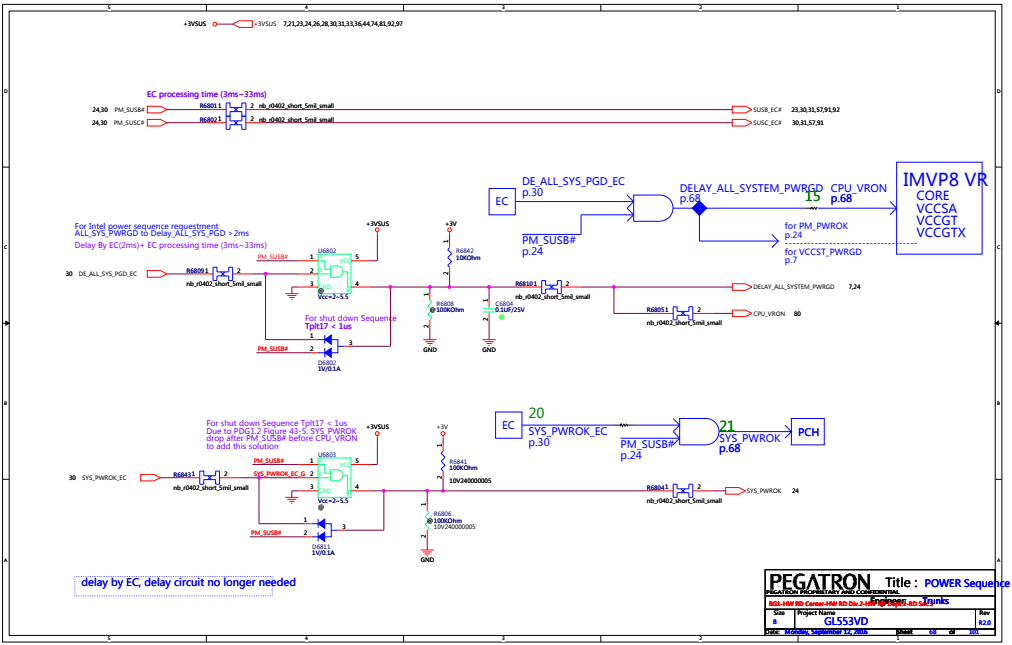


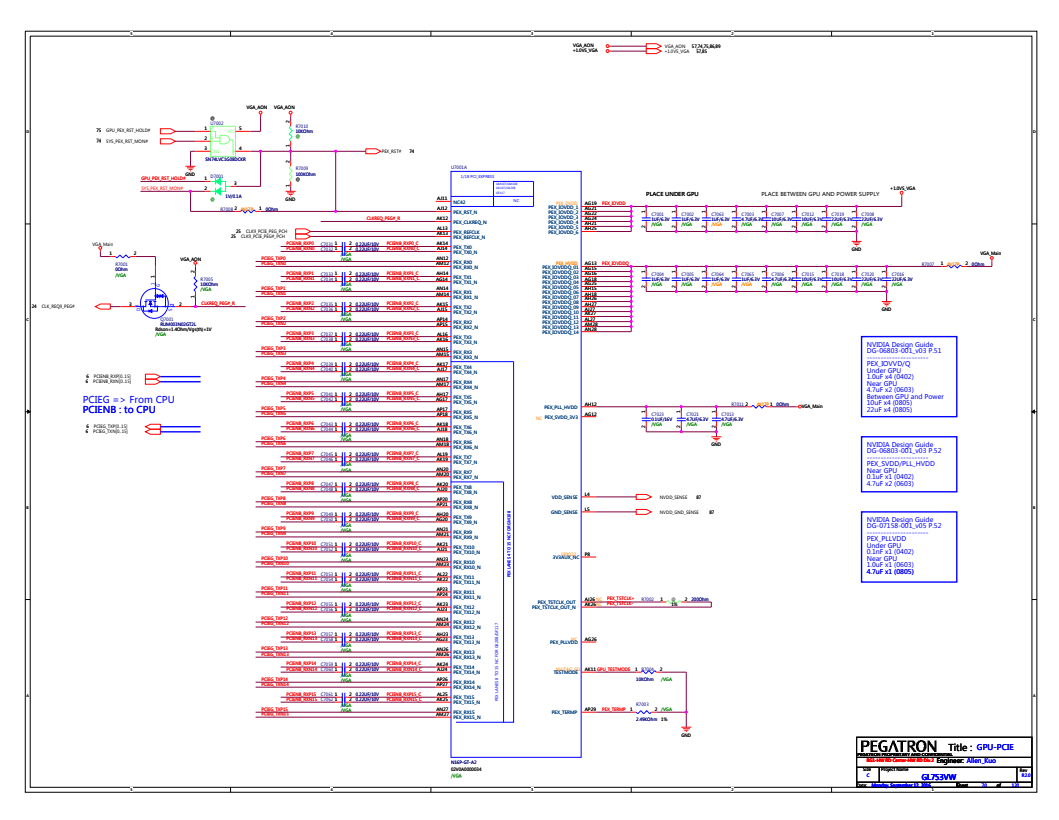
Hall sensor Conn. (MB SIDE)

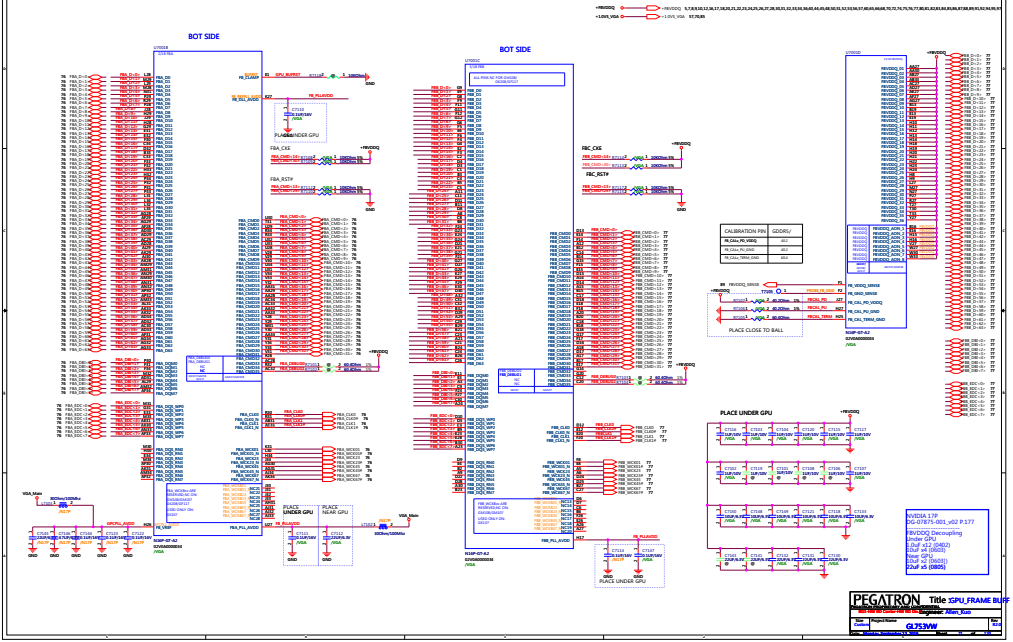


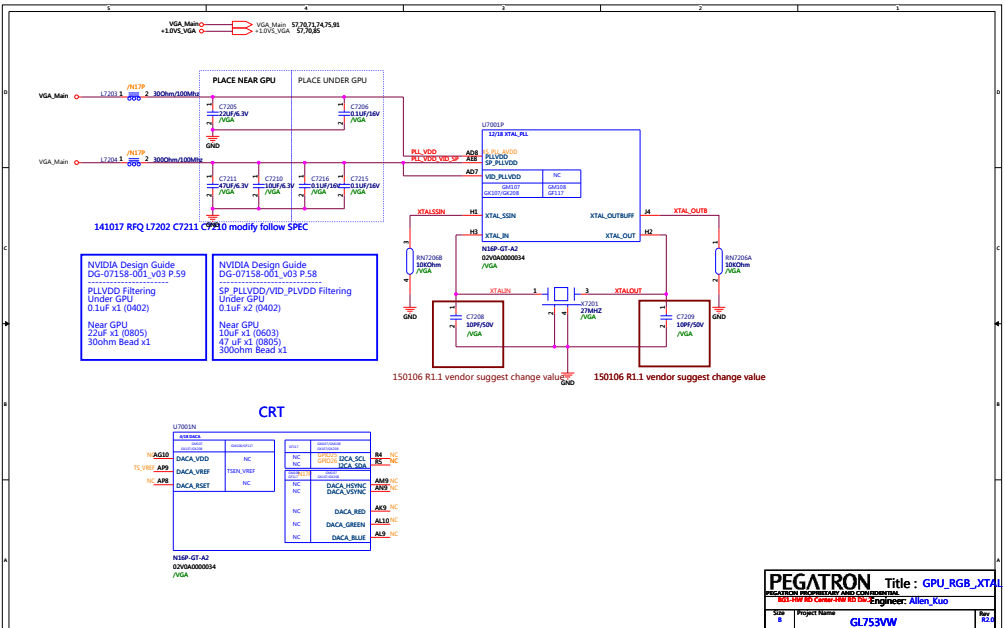


PEGATRON	Title :	IO BOARD CON	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
	Engineer:	Trunks	
Size: B	Project Name: GL553VD		Rev: RA0
Date: Monday, September 12, 2016	Sheet: 66 of 108		

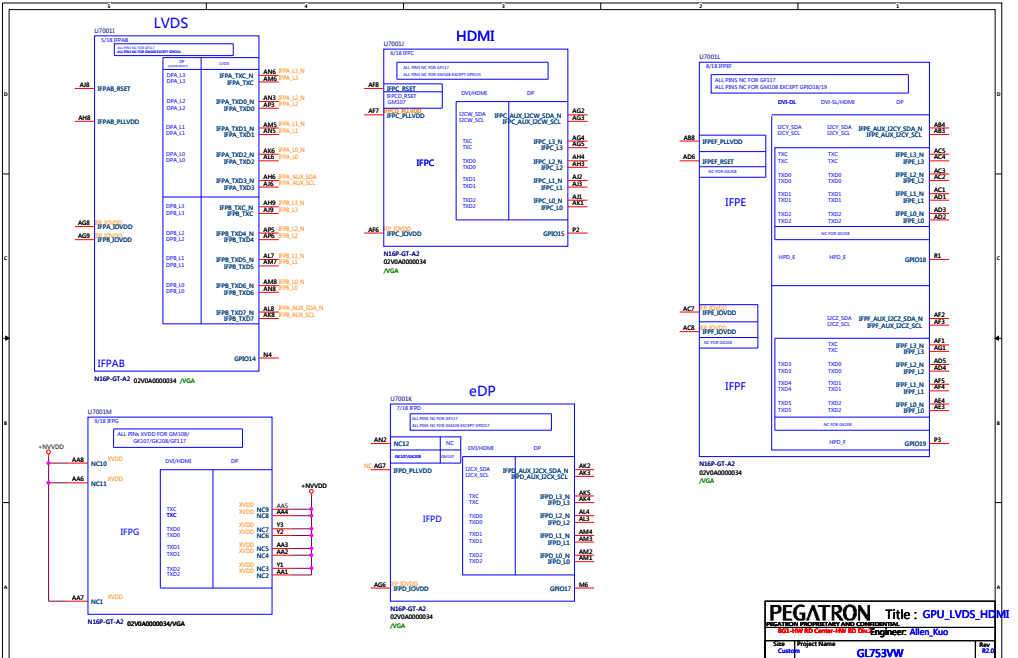

+3VSUS
+3VSUS 7,21,23,24,26,28,30,31,33,36,44,74,81,92,97
EC processing time (3ms~33ms)
24,30 PM_SUSB#
R6801 1 2 nb_r0402_short_5mil_small
SUSB_EC# 23,30,31,57,91,92
24,30 PM_SUSC#
R6802 1 2 nb_r0402_short_5mil_small
SUSC_EC# 30,31,57,91
EC
DE_ALL_SYS_PGD_EC
p.30
DELAY_ALL_SYSTEM_PWRGD
p.68
15
CPU_VRON
p.68
PM_SUSB#
p.24
for PM_PWROK
p.24
for VCCST_PWRGD
p.7
IMVP8 VR
CORE
VCCSA
VCCGT
VCCGTX
For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD > 2ms
Delay By EC(2ms)+ EC processing time (3ms~33ms)
30 DE_ALL_SYS_PGD_EC
R6809 1 2 nb_r0402_short_5mil_small
U6802
PM_SUSB#
VCC
GND
Vcc=2~5.5
+3VSUS
+3V
R6842 1 2 10KOhm
R6808 1 2 @ 100KOhm
GND
C6804 0.1UF/25V
GND
R6810 1 2 nb_r0402_short_5mil_small
DELAY_ALL_SYSTEM_PWRGD 7,24
R6805 1 2 nb_r0402_short_5mil_small
CPU_VRON 80
For shut down Sequence
Tpl17 < 1us
PM_SUSB#
D6802
1V/0.1A
For shut down Sequence Tpl17 < 1us
Due to PDG1.2 Figure 43-5 SYS_PWROK
drop after PM_SUSB# before CPU_VRON
to add this solution
EC
20
SYS_PWROK_EC
p.30
PM_SUSB#
p.24
21
SYS_PWROK
p.68
PCH
30 SYS_PWROK_EC
R6843 1 2 nb_r0402_short_5mil_small
U6803
PM_SUSB#
SYS_PWROK_EC_G
VCC
GND
Vcc=2~5.5
+3V
R6841 1 2 100KOhm
10V2400000005
R6806 1 2 @ 100KOhm
10V2400000005
GND
R6804 1 2 nb_r0402_short_5mil_small
SYS_PWROK 24
PM_SUSB#
D6811
1V/0.1A
delay by EC, delay circuit no longer needed
PEGATRON
Title : POWER Sequence
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer:
BG1-HW RD Center-HW RD Div.2-HW RD Sec.5-Chunks
Size: A
Project Name: GL553VD
Rev: R2.0
Date: Monday, September 14, 2015
Sheet 68 of 104


PCIEG => From CPU
PCIEN8 : to CPU
PLACE UNDER GPU
PLACE BETWEEN GPU AND POWER SUPPLY
NVIDIA Design Guide
DG-06803-001_v03 P.51
PEX_IOVV/IOVD
Under GPU
1.0uF x4 (0402)
Near GPU
4.7uF x2 (0603)
Between GPU and Power
10uF x4 (0805)
22uF x4 (0805)
NVIDIA Design Guide
DG-06803-001_v03 P.52
PEX_SVDD/PLL_HVDD
Near GPU
0.1uF x1 (0402)
1.0uF x2 (0603)
NVIDIA Design Guide
DG-07138-001_v03 P.52
PEX_PLLVDD
Under GPU
0.1nF x1 (0402)
Near GPU
1.0uF x1 (0603)
4.7uF x1 (0805)
PEGATRON
Title : GPU-PCIE
GL753VW

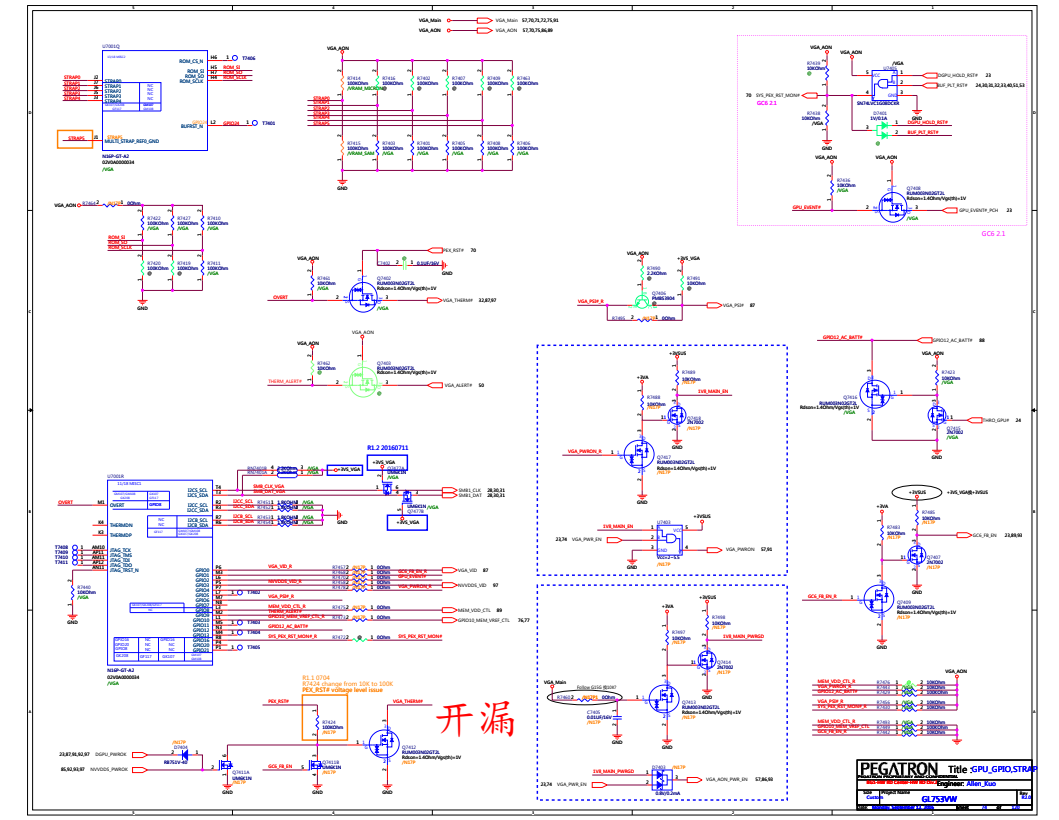

BOT SIDE
BOT SIDE
PLACE UNDER GPU
PLACE NEAR GPU
PLACE UNDER GPU
PLACE CLOSE TO BALL
PLACE UNDER GPU
PLACE UNDER GPU
CALIBRATION PIN GD0/EU
PR_Data_PU_VDD 49.2
PR_Data_PU_GND 49.2
PR_Data_TRIM_GND 60.4
NVIDIA 179
SG-07875-003_v02 P.177
HW/DDQ Decoupling
Under GPU
1.0uF x4 (0402)
2.2uF x4 (0603)
Near GPU
1.0uF x2 (0603)
22uF x5 (0805)
PEGATRON
Title :GPU_FRAME BUFF
Engineer: Allen_Kuo
GL753VW

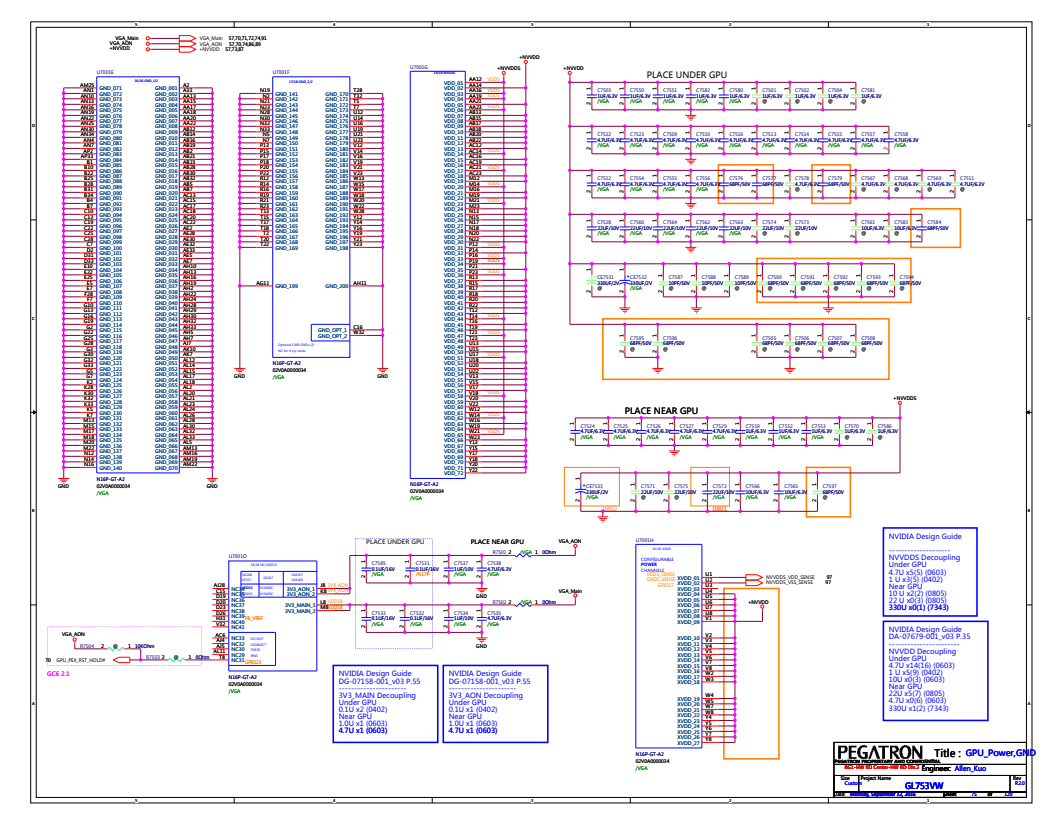


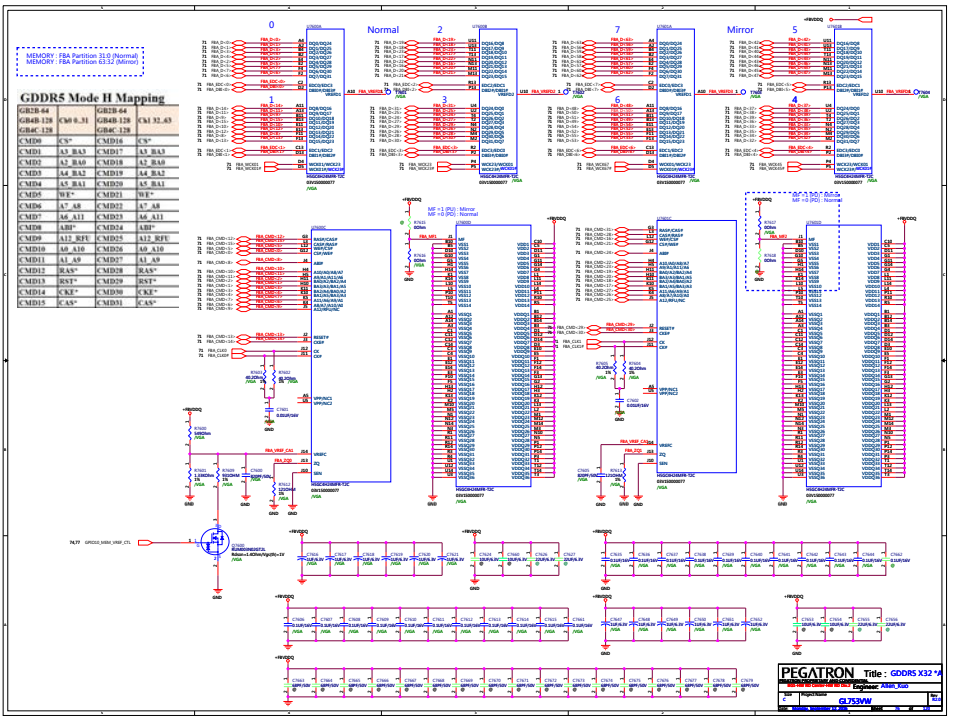
PEGATRON	Title : GPU_RGB_XTAL	
PEGATRON PROPRIETARY AND CONFIDENTIAL		
R03-HW RD Center-HW RD Div.	Engineer: Allen_Kuo	
Size: B	Project Name: GL753VW	Rev: R2.0
Date: Monday, September 12, 2016	Sheet: 72 of 120	

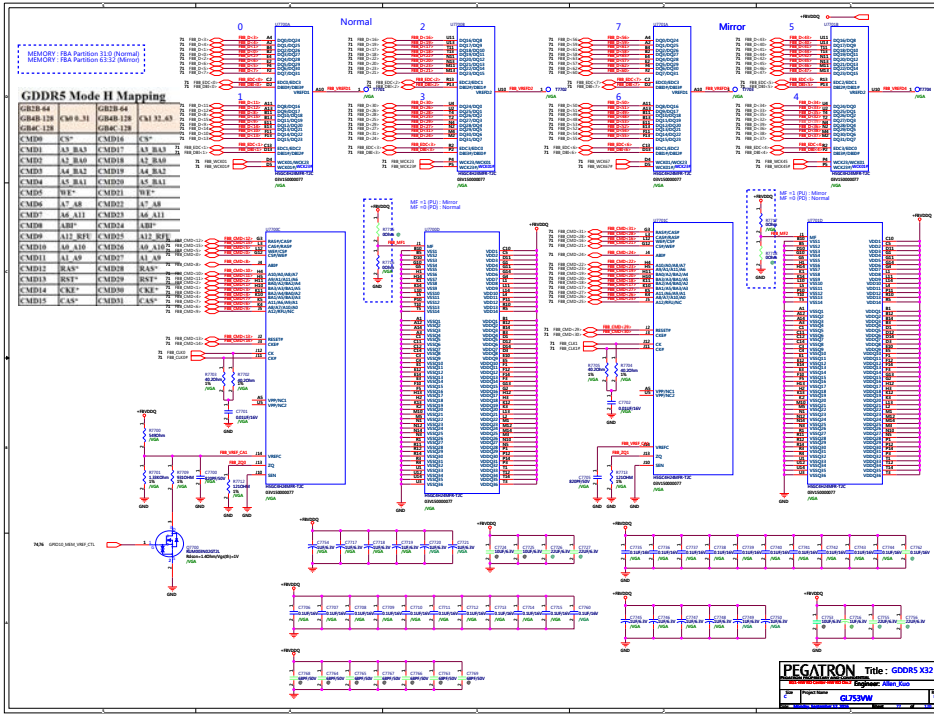


PEGATRON	Title : GPU_LVDS_HDMI		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
R01-HW BS Center-HW BS Dep.	Engineer: Allen_Kuo		
Site: Custom	Project Name: GL753VW		Rev: 82.0
Date: Monday, September 12, 2016	Sheet: 73 of 120		

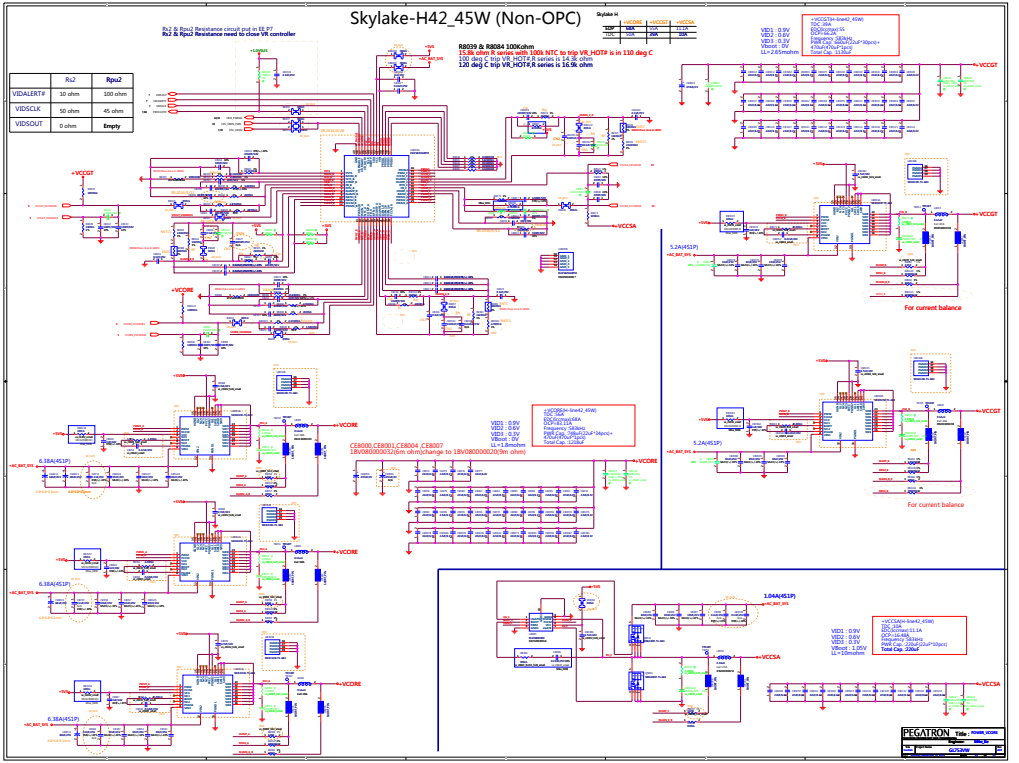

开漏
R1.1 0704
R742.4 change from 10K to 100K
PEX_RST# voltage level issue
R1.2 20160711
+3VS_VGA
PEGATRON
Title :GPU_GPIO,STRAP
Engineer: Allen_Kuo
GL75VW

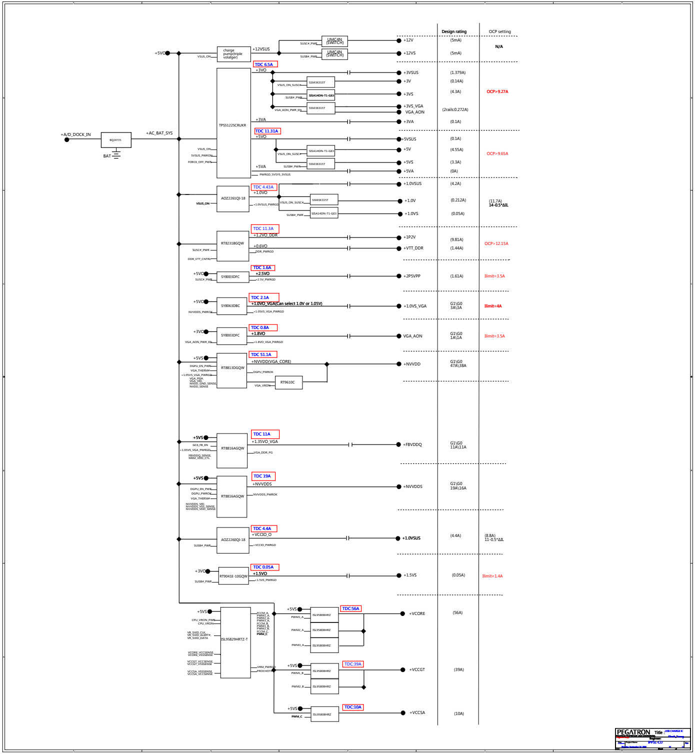

PLACE UNDER GPU
PLACE NEAR GPU
NVIDIA Design Guide
DG-07158-001_v03 P.35
3V3_MAIN Decoupling
Under GPU
0.1U x2 (0402)
Near GPU
1.0U x1 (0603)
4.7U x1 (0603)
NVIDIA Design Guide
DG-07158-001_v03 P.35
3V3_AON Decoupling
Under GPU
0.1U x1 (0402)
Near GPU
1.0U x1 (0603)
4.7U x1 (0603)
NVIDIA Design Guide
DA-07679-001_v03 P.35
NVVDD Decoupling
Under GPU
4.7U x5(6) (0603)
1 U x5(9) (0402)
330 u(3) (0603)
Near GPU
22U x5(7) (0805)
4.7U x6(6) (0603)
330U x1(2) (7343)
PEGATRON
Title : GPU_Power,GND
Engineer: Allen_Kuo
Size: Custom
Project Name: GL753VW
Rev: 0.1A
Date: Monday, September 22, 2014
Sheet: 26 of 48


MEMORY : FBA Partition 31:0 (Normal)
MEMORY : FBA Partition 63:32 (Mirror)
GDDR5 Mode H Mapping
GB2B-64
GB4B-128
GB4C-128
Ch0 31:0
Ch1 32:63
CMD0
CS*
CMD16
CS*
CMD1
A3 BA3
CMD17
A3 BA3
CMD2
A2 BA0
CMD18
A2 BA0
CMD3
A4 BA2
CMD19
A4 BA2
CMD4
A5 BA1
CMD20
A5 BA1
CMD5
WE*
CMD21
WE*
CMD6
A7 A8
CMD22
A7 A8
CMD7
A6 A11
CMD23
A6 A11
CMD8
ABI*
CMD24
ABI*
CMD9
A12 RFU
CMD25
A12 RFU
CMD10
A0 A10
CMD26
A0 A10
CMD11
A1 A9
CMD27
A1 A9
CMD12
RAS*
CMD28
RAS*
CMD13
RST*
CMD29
RST*
CMD14
CKE*
CMD30
CKE*
CMD15
CAS*
CMD31
CAS*
Normal
Mirror
0
1
2
3
4
5
6
7
MF =1 (PU) : Mirror
MF =0 (PD) : Normal
PEGATRON
Title : GDDR5 X32 *2
Engineer: Adam_Kuo
GJ.753VW


MEMORY : FBA Partition 31:0 (Normal)
MEMORY : FBA Partition 63:32 (Mirror)
GDDR5 Mode H Mapping
GB2B-64
GB4B-128 Ch0 0..31
GB4B-128 Ch1 32..63
GB4C-128
CMD0 CS*
CMD1 A5 BA3
CMD2 A2 BA0
CMD3 A4 BA2
CMD4 A5 BA1
CMD5 WE*
CMD6 A7 A8
CMD7 A6 A11
CMD8 ABI*
CMD9 A12_RFU
CMD10 A0_A10
CMD11 A1 A9
CMD12 RAS*
CMD13 RST*
CMD14 CKE*
CMD15 CAS*
GB2B-64
GB4B-128 Ch0 0..31
GB4B-128 Ch1 32..63
GB4C-128
CMD0 CS*
CMD1 A3 BA3
CMD2 A3 BA0
CMD3 A4 BA2
CMD4 A5 BA1
CMD5 WE*
CMD6 A7 A8
CMD7 A6 A11
CMD8 ABI*
CMD9 A12_RFU
CMD10 A0_A10
CMD11 A1 A9
CMD12 RAS*
CMD13 RST*
CMD14 CKE*
CMD15 CAS*
Normal
Mirror
MF =1 (FU) : Mirror
MF =0 (PD) : Normal
PEGATRON
Title : GDDR5 X32 *R
Engineer: Allen_Kuo
Project Name
GL753VW

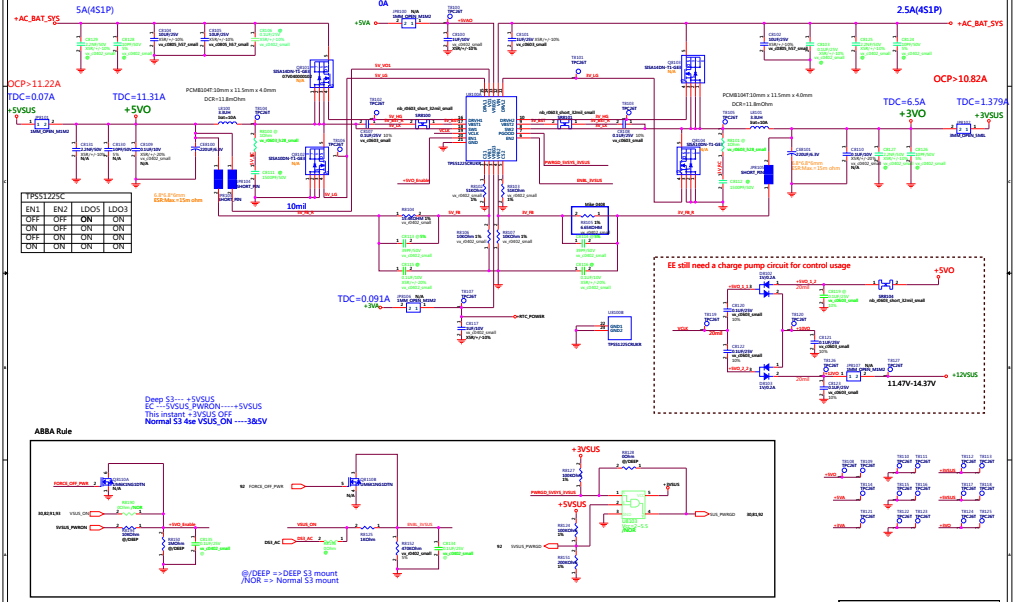
Skylake-H42_45W (Non-OPC)



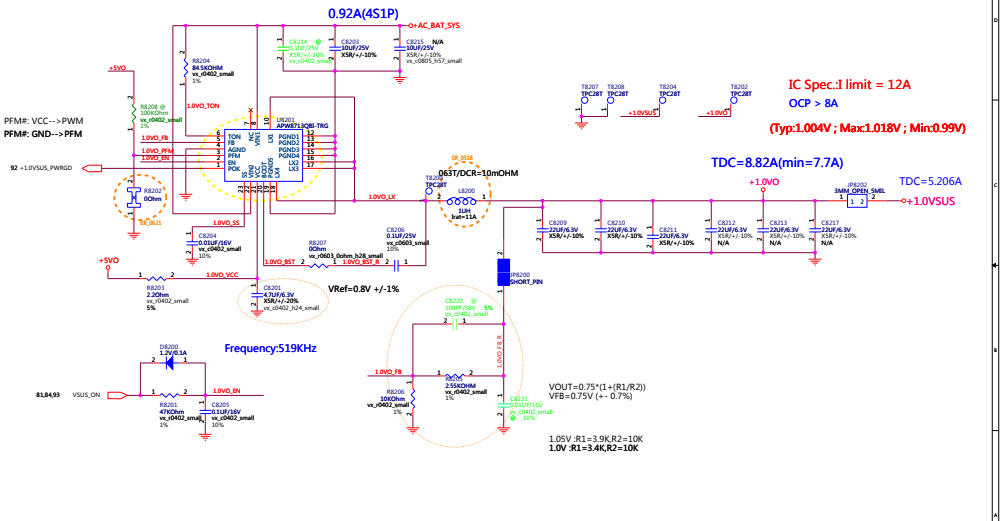


Design rating
OCP setting
+A/D_DOCK_IN
BQ24735
BAT
+AC_BAT_SYS
+5VO
charge pump(triple volatger)
+12VSUS
UMC4N (SWITCH)
+12V
+12VS
(5mA)
N/A
TPS51225CRUKR
TDC 6.5A
+3VO
+3VSUS
+3V
+3VS
+3VS_VGA
VGA_AON
+3VA
(1.379A)
(0.14A)
(4.3A)
(2rails:0.272A)
(0.1A)
OCP>9.27A
TDC 11.31A
+5VO
+5VSUS
+5V
+5VS
+5VA
(0.1A)
(4.55A)
(3.3A)
(0A)
OCP>9.65A
AOZ2261QI-18
TDC 4.43A
+1.0VO
+1.0VSUS
+1.0V
+1.0VS
(4.2A)
(0.212A)
(0.05A)
(11.7A)
14-0.5*ΔIL
RT8231BGQW
TDC 11.3A
+1.2VO_DDR
+0.6VO
+1P2V
+VTT_DDR
(9.81A)
(1.44A)
OCP>12.15A
SY8003DFC
TDC 1.6A
+2.5VO
+2P5VPP
(1.61A)
Ilimit=3.5A
SY8063DBC
TDC 2.1A
+1.0VO_VGA(Can select 1.0V or 1.05V)
+1.0VS_VGA
G1\G0 3A\3A
Ilimit=4A
SY8003DFC
TDC 0.8A
+1.8VO
VGA_AON
G1\G0 1A\1A
Ilimit=3.5A
RT8813DGQW
TDC 51.1A
+NVVDD(VGA_CORE)
RT9610C
+NVVDD
G1\G0 47A\38A
RT8816AGQW
TDC 11A
+1.35VO_VGA
+FBVDDQ
G1\G0 11A\11A
RT8816AGQW
TDC 19A
+NVVDDS
+NVVDDS
G1\G0 19A\16A
AOZ2260QI-18
TDC 4.4A
+VCCIO_O
+1.0VSUS
(4.4A)
(8.8A)
11-0.5*ΔIL
RT9041E-10GQW
TDC 0.05A
+1.5VO
+1.5VS
(0.05A)
Ilimit=1.4A
ISL95829HRTZ-T
ISL95808HRZ
TDC:56A
+VCORE
(56A)
TDC:39A
+VCCGT
(39A)
TDC:10A
+VCCSA
(10A)
PEGATRON
Title :

+5VO & +3VO POWER SUPPLY

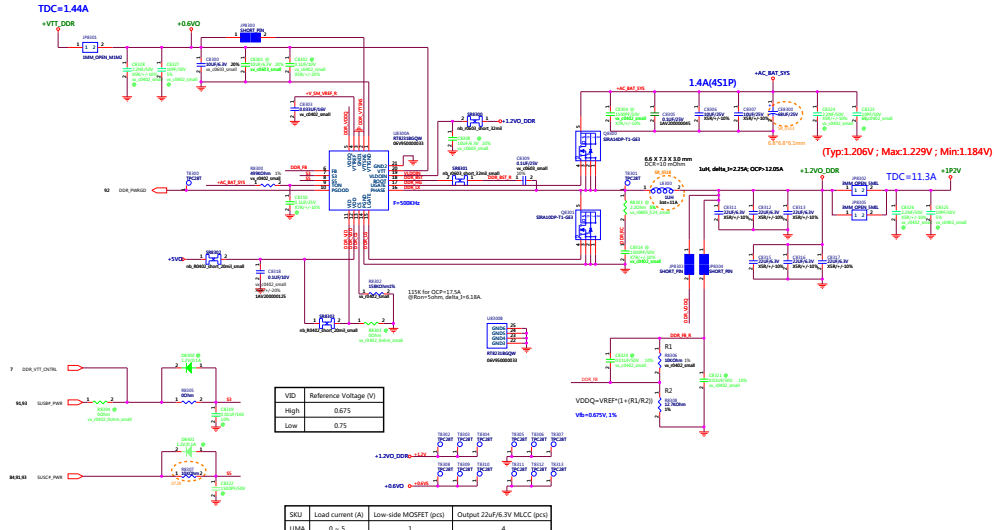


1.0VSUS POWER SUPPLY



PEGATRON	Title :	POWER_+1.0VSUS	
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer:	Benson_Lin	
Size: A3	Project Name	GL553VW	Rev
Date: Monday, September 12, 2016	Sheet	82	of 94

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

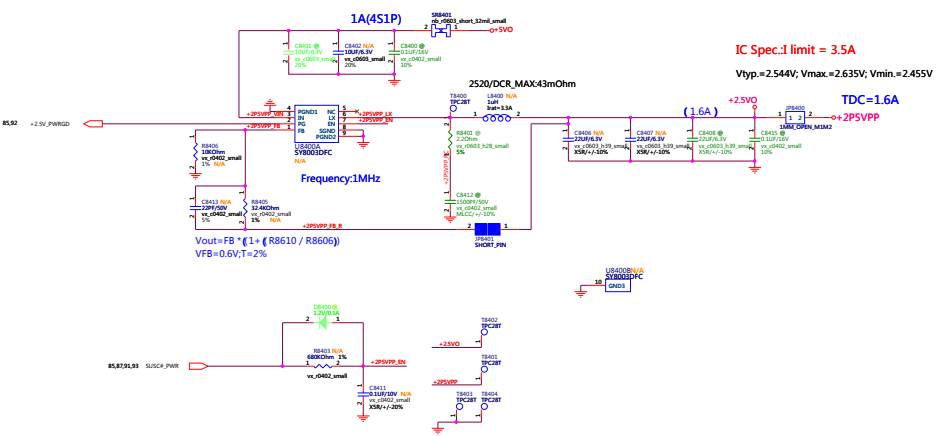
PEGATRON Title : POWER_DDR & VTT

Engineer: Ramsan_Lin

Size: Project Name: GL553VW Rev: 1A

Monday, September 15, 2014 Sheet 41 of 45

+2.5V POWER SUPPLY



PEGATRON	Title : POWER_2.5VPP & 1.5VS		
Size	Project Name	GL553VW	Rev
	Monday, September 12, 2016	Sheet 84 of 94	

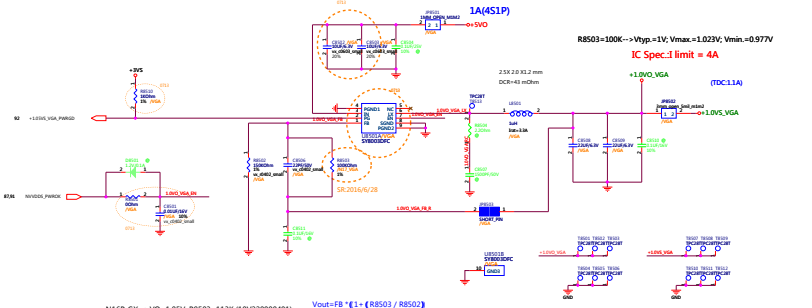
1.0VS_VGA(+1P0V_GPU) POWER SUPPLY

R8503 need to change Voltage 1V & 1.05V

+1.0VS_VGA

	N16P-GX	N17P-G1
EDP	2.9A	TBD
TDC	2.57A	3A
Voltage	1.05V	1V

R8503=113K-->Vtyp.=1.052V; Vmax.=1.077V; Vmin.=1.027V



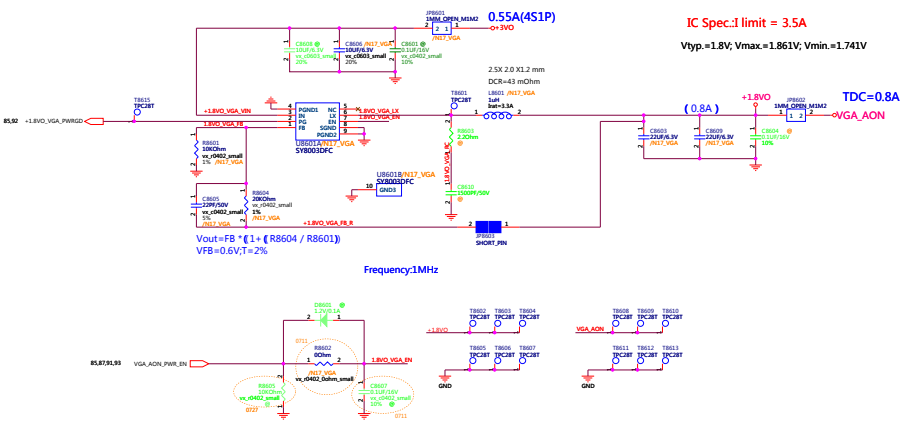
PEGATRON Title : +POWER_+1.0VS_VGA

Engineer: Ranson_Lin

Size: Project Name: GL553VW Rev:

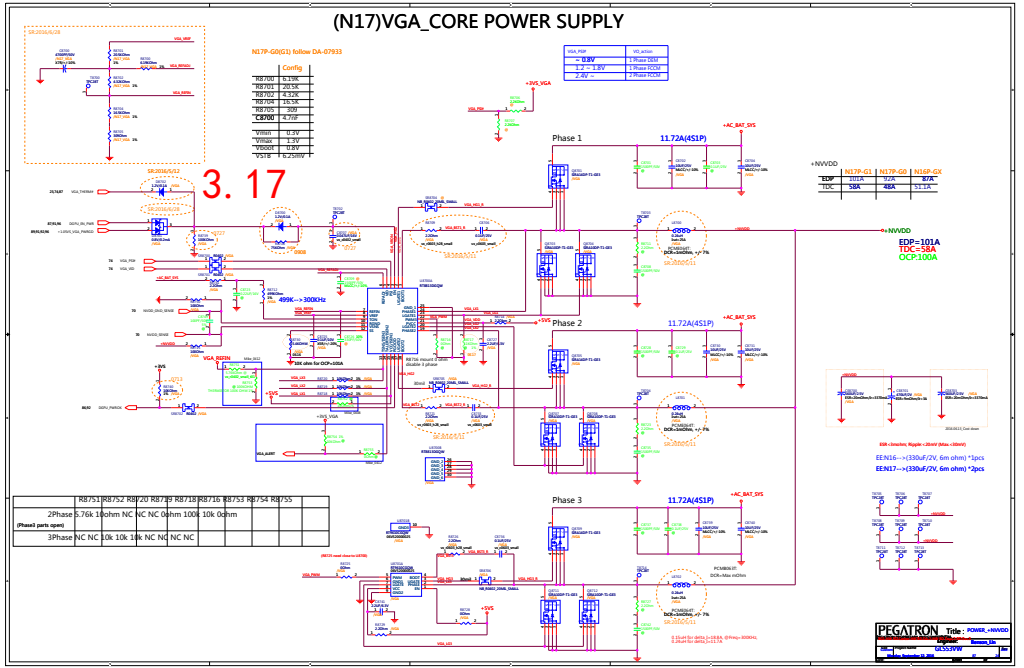
Date: Monday, December 19, 2016 Sheet of

+1.8V POWER SUPPLY



PEGATRON	Title :	POWER_1.8V0(VGA_AON)	
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer:	Benson_Lin	
Size:	Project Name	GL553VW	Rev
Date: Monday, September 12, 2016	Sheet	36 of 74	

(N17)VGA_CORE POWER SUPPLY



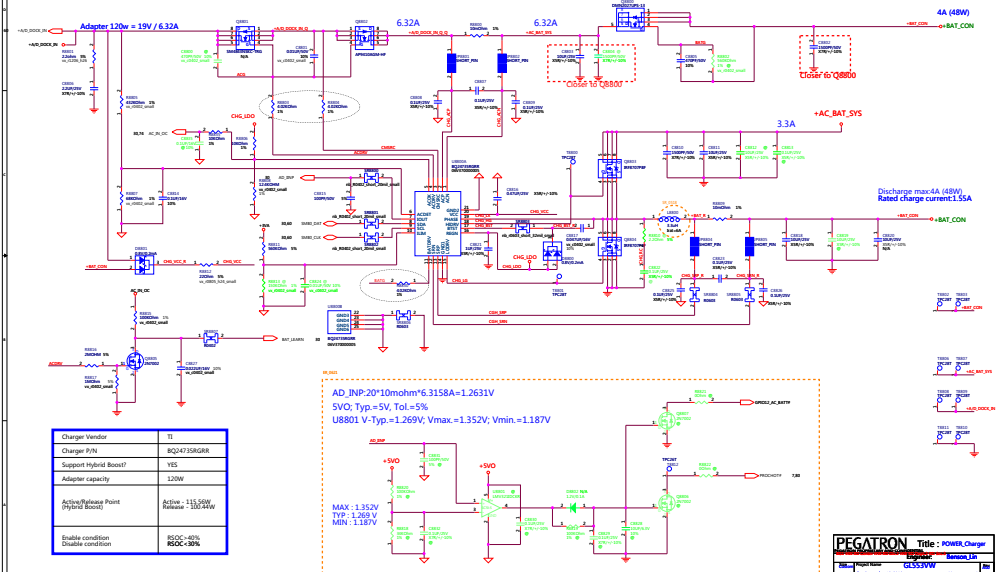
Config	
R8700	6.19K
R8701	20.5K
R8702	4.32K
R8704	16.5K
R8705	30K
C8700	4.7nF
Vtrim	0.2V
Vtrim2	1.3V
Vboot	0.8V
Vslf	1.625mV

VGA_PSP	VG_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase PCM
2.4V ~	2 Phase PCM

	R8751	R8752	R8720	R8719	R8718	R8716	R8753	R8754	R8755	
2Phase (Phase3 parts open)	5.76K	10ohm	NC	NC	NC	0ohm	100k	10k	0ohm	
3Phase	NC	NC	10k	10k	10k	NC	NC	NC	NC	

	N17P-G1	N17P-G0	N16P-GX
EDP	101A	92A	87A
TDC	58A	48A	51.1A

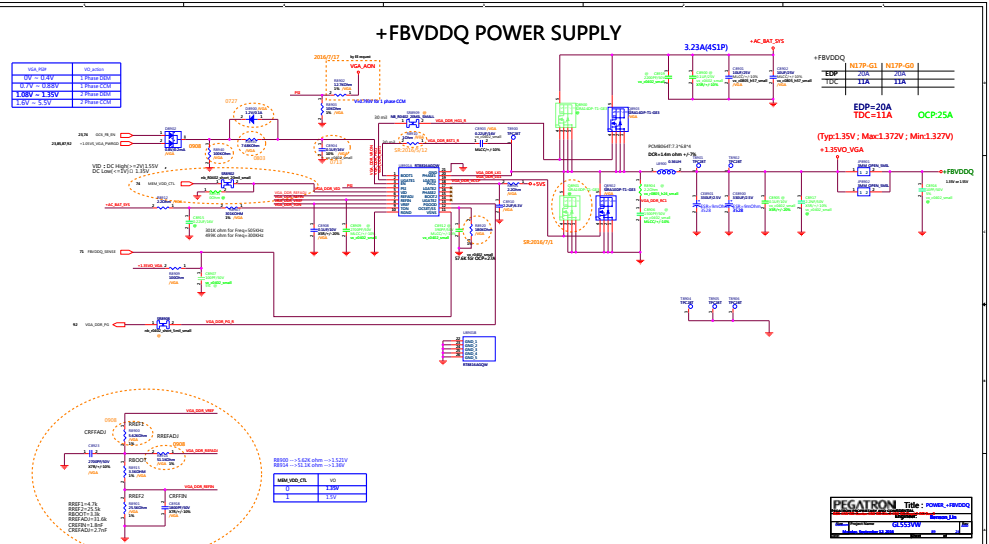
BATTERY CHARGER



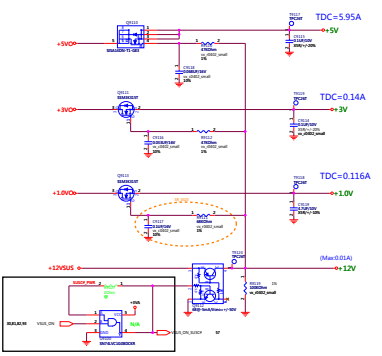
Charger Vendor	TI
Charger P/N	BQ24735RGRR
Support Hybrid Boost?	YES
Adapter capacity	120W
Active/Release Point (Hybrid Boost)	Active - 115.56W Release - 100.44W
Enable condition Disable condition	RSOC<40% RSOC<30%

PEGATRON	Title : POWER_Charger		
	Engineer:	Benson_Lin	
	GL553VW		Rev
	Wednesday, September 16, 2015	Sheet	35 of

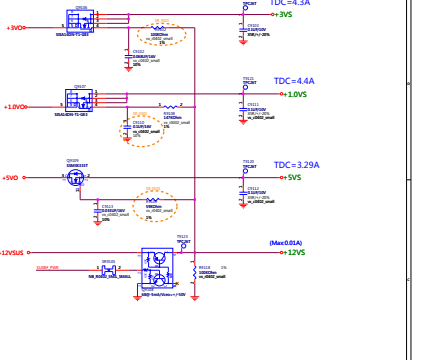
+FBVDDQ POWER SUPPLY



SUSC#_PWR POWER



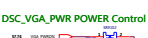
SUSB#_PWR POWER

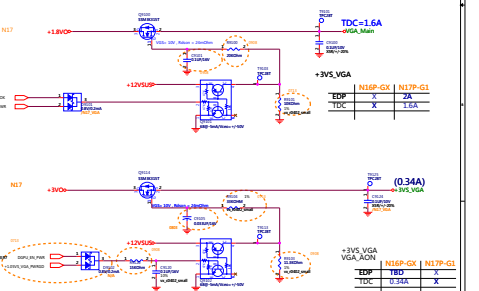


SUSB#_PWR POWER Control

SUSC#_PWR POWER Control

DSC_VGA_PWR POWER Control

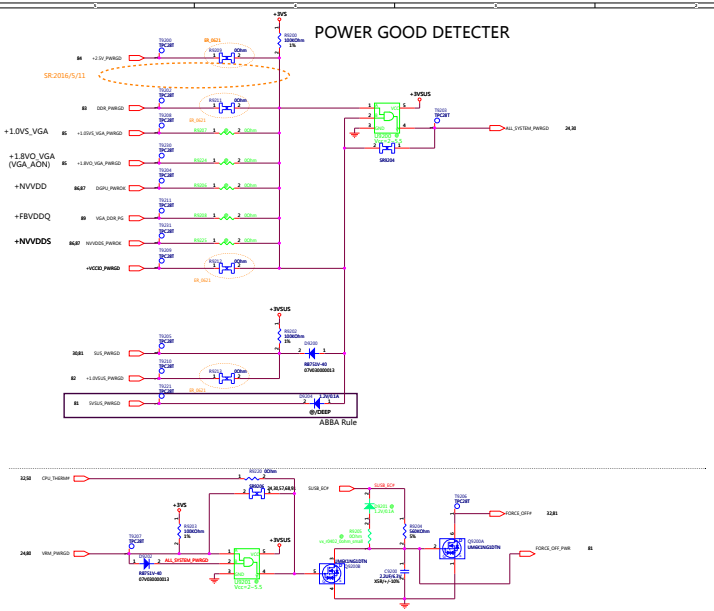




PEGATRON Title: POWER_Load Switch

Size: Project Name: QIS53.3VW Rev:

Date: Sheet of



PEGATRON	Title :	POWER_Protect	
	Engineer:	Benson_Lin	
Size	Project Name	GL553VW	Rev
	Monday, November 23, 2015	Sheet	of

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,84,87,88,89,95

+BAT_CON → +BAT_CON 60,88

+5VA → +5VA 81

+3VA → +3VA 25,30,57,60,81,88,91,101

+5VO → +5VO 81,82,83,88,91

+3VO → +3VO 81,85,86,91

+1.5VO → +1.5VO

+5VSUS → +5VSUS 36,51,56,81

+3VSUS → +3VSUS 7,21,23,24,26,28,30,33,36,68,81,92

+3V → +3V 24,40,45,53,57,68,91

+5VS → +5VS 36,48,50,51,56,57,80,87,89,91,95

+3VS → +3VS 7,16,17,21,22,23,24,26,28,30,31,32,33,36,44,45,48,50,51,57,91,92

+1.5VS → +1.5VS 36

+VCORE → +VCORE 9,80

+VCCIO → +VCCIO 3,6,7,10

FOR POWER TEST

+3VA

JP9300 @ SGL_JUMP → T9300 TPC28T → CPU_VRON_PWR 80

JP9301 @ SGL_JUMP → T9301 TPC28T → SUSB#_PWR 83,91

JP9302 @ SGL_JUMP → T9302 TPC28T → SUSC#_PWR 83,84,91

JP9303 @ SGL_JUMP → T9303 TPC28T → VSUS_ON 30,81,82,91

VCCIO +1.5VS

JP9304 @ SGL_JUMP → T9304 TPC28T → SVSUS_PWRON 30,81,82,91

5VO

JP9305 @ SGL_JUMP → T9305 TPC28T → DDR_VTT_CNTRL 30,81,82,91

VTT

JP9306 @ SGL_JUMP → T9306 TPC28T → NVVDDS_PWROK 30,81,82,91

+1.0VS_VGA

JP9307 @ SGL_JUMP → T9307 TPC28T → VGA_AON_PWR_EN 30,81,82,91

+1.8V_VGA_AON +NVVDDS

JP9308 @ SGL_JUMP → T9308 TPC28T → DGPU_EN_PWR 30,81,82,91

+NVVDD

JP9309 @ SGL_JUMP → T9309 TPC28T → GC6_FB_EN 30,81,82,91

+FBVDDQ

PEGATRON

Title : POWER_Signal

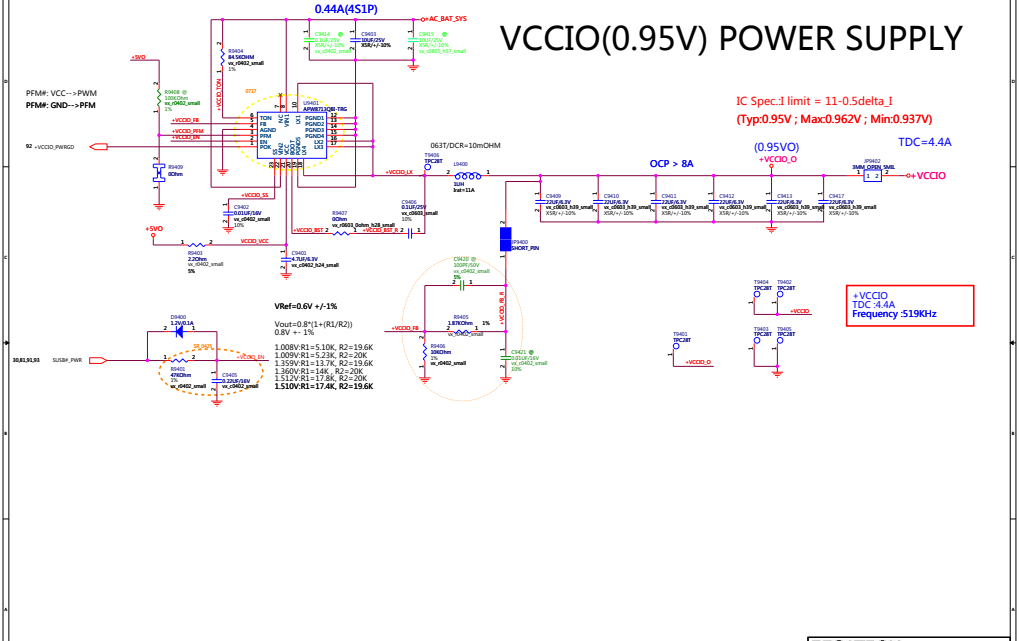
Engineer: Benson_Lin

Size: Custom | Project Name: GL553VW | Rev: 3A6

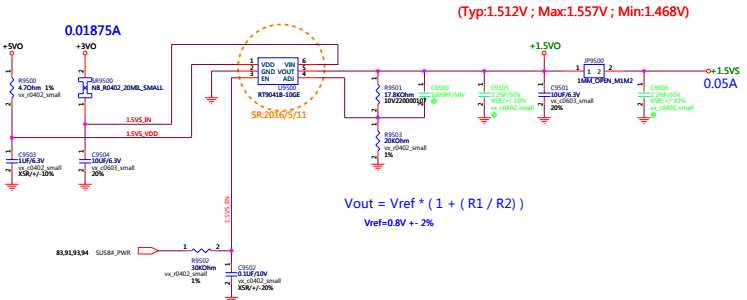
Monday, September 12, 2016 | Sheet 93 of 24

Date: | Sheet | of

VCCIO(0.95V) POWER SUPPLY

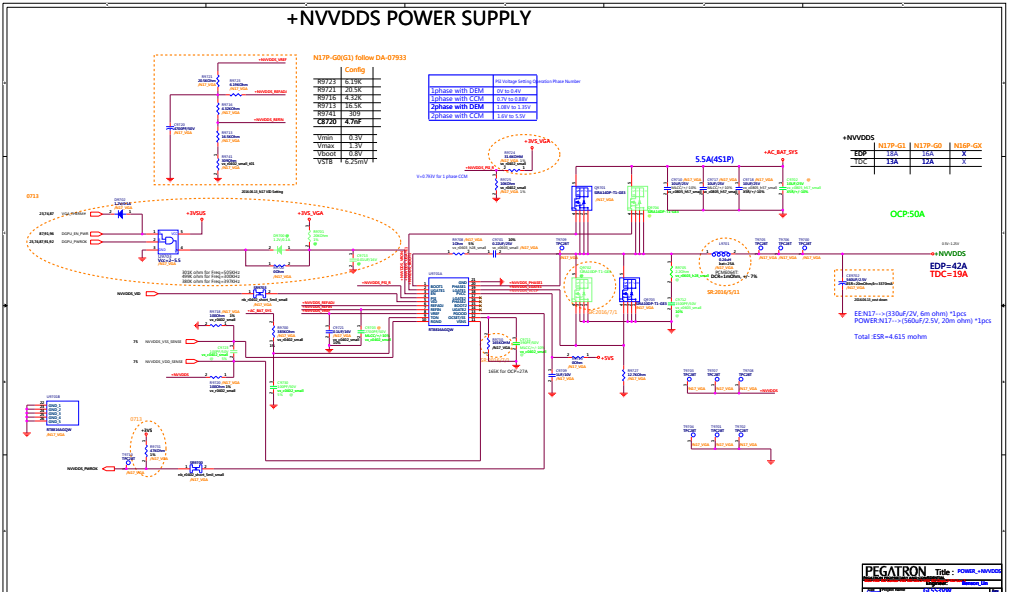


1.5V POWER SUPPLY

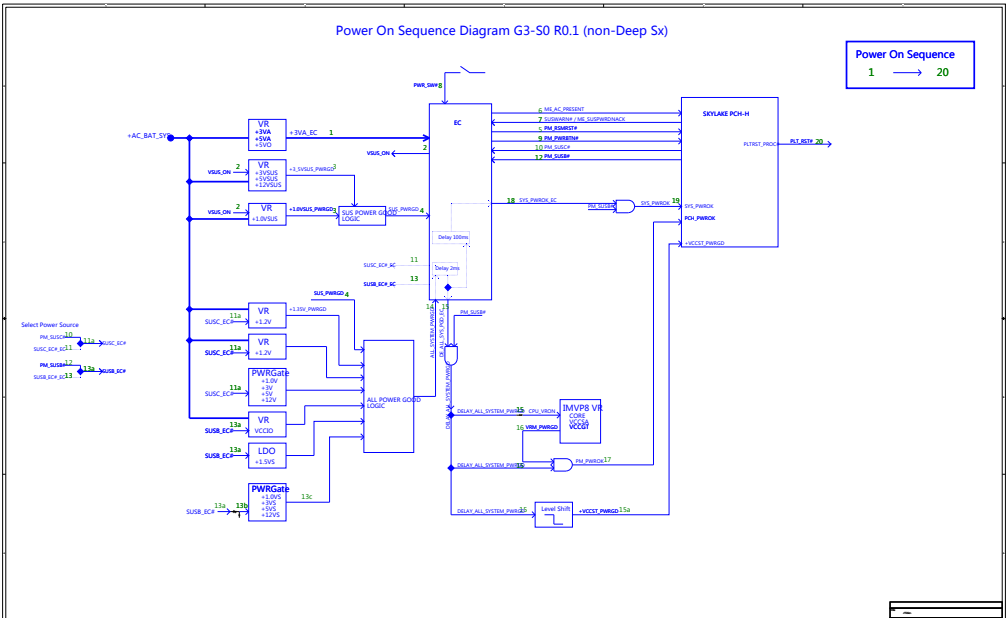


PEGATRON	Title : POWER_1.5VS	
PEGATRON PROPRIETARY AND CONFIDENTIAL		
	Engineer: Benson_Lin	
Size	Project Name	Rev
	GL553VW	
Date: Monday, September 12, 2016	Sheet 95 of 24	

+NVVDDS POWER SUPPLY



Power On Sequence Diagram G3-S0 R0.1 (non-Deep Sx)



USB2.0 on DB

To MB

TYPE A
phi 8 drill 3

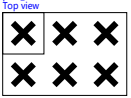
NPTH_2.5phi

NPTH_2.5 x 2.9 phi

PEGATRON	Title : IO_Small_BD	
	Engineer: Bernie Huang	
Size: B	Project Name: GL553VD	Rev: R2.0
Date: Monday, September 12, 2016	Sheet 100 of 99	

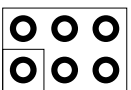
LID Switch

pin1_DB
Top view



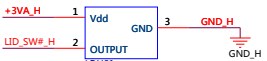
LDJ01
pin1:LID_SW#_H
pin3:GND_H
pin5:+3VA_H

CON6602
pin2:LID_SW#
pin4:GND
pin6:+3VA

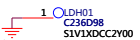


pin1_MB
Top view

HEADER_2X3P
12V06GBSD016



phi 6 drill 2.5



Tooling hole
2 x 2p2

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: Hall Sensor Board
Engineer: Bernie Huang
BG1-HW RD Center-HW RD Div.2-HW RD Dept1-RD Sec.7

Size	Project Name	Rev
A	GL553VD	R2.0

Date: Monday, September 12, 2016 Sheet 101 of 99